

SN74LVC2G125 Dual Bus Buffer Gate With 3-State Outputs

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.3 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Max of 5.5 V Down to the V_{CC} Level
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

2 Applications

- Cable Modem Termination Systems
- High-Speed Data Acquisition and Generation
- Military: Radars and Sonars
- Motor Controls: High-Voltage
- Power Line Communication Modems
- SSDs: Internal or External
- Video Broadcasting and Infrastructure: Scalable Platforms
- Video Broadcasting: IP-Based Multi-Format Transcoders
- Video Communications Systems

3 Description

The SN74LVC2G125 device is a dual bus buffer gate, designed for 1.65-V to 5.5-V V_{CC} operation. This device features dual line drivers with 3-state outputs. The outputs are disabled when the associated output-enable (\overline{OE}) input is high.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC2G125	SM8 (8)	2.95 mm x 2.80 mm
	US8 (8)	2.30 mm x 2.00 mm
	DSBGA (8)	1.91 mm x 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

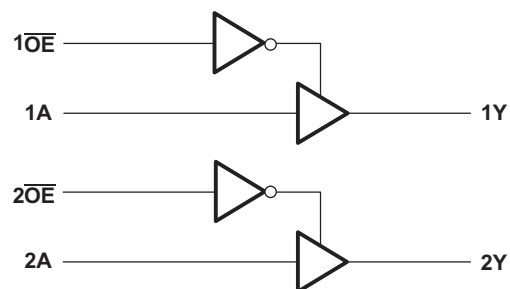


Table of Contents

1 Features	1	8.1 Overview	9
2 Applications	1	8.2 Functional Block Diagram	9
3 Description	1	8.3 Feature Description	9
4 Revision History	2	8.4 Device Functional Modes	9
5 Pin Configuration and Functions	3	9 Application and Implementation	10
6 Specifications	4	9.1 Application Information	10
6.1 Absolute Maximum Ratings	4	9.2 Typical Application	10
6.2 ESD Ratings	4	10 Power Supply Recommendations	11
6.3 Recommended Operating Conditions	5	11 Layout	11
6.4 Thermal Information	5	11.1 Layout Guidelines	11
6.5 Electrical Characteristics	6	11.2 Layout Example	11
6.6 Switching Characteristics	6	12 Device and Documentation Support	12
6.7 Switching Characteristics	6	12.1 Trademarks	12
6.8 Operating Characteristics	7	12.2 Electrostatic Discharge Caution	12
6.9 Typical Characteristics	7	12.3 Glossary	12
7 Parameter Measurement Information	8	13 Mechanical, Packaging, and Orderable Information	12
8 Detailed Description	9		

4 Revision History

Changes from Revision O (January 2015) to Revision P

Page

- Added overbar for active low to $\overline{1OE}$ and $\overline{2OE}$ to the *Simplified Schematic*..... **1**
- Added T_J Junction temperature to the *Absolute Maximum Ratings*
- Added overbar for active low to $\overline{1OE}$ and $\overline{2OE}$ to the *Functional Block Diagram*..... **9**

Changes from Revision N (November 2013) to Revision O

Page

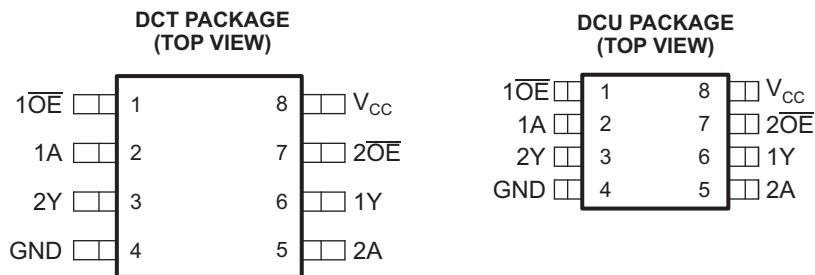
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. **1**

Changes from Revision M (January 2007) to Revision N

Page

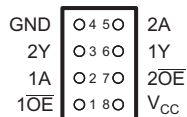
- Updated document to new TI data sheet format. **1**
- Removed Ordering Information table. **1**
- Updated *Features*. **1**
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. **5**
- Added ESD warning. **12**

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

YZP PACKAGE (BOTTOM VIEW)



See mechanical drawings for dimensions.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DCT, DCU, YZP		
1A	2	I	Input
2A	5	I	Input
1OE	1	I	Output Enable for buffer 1
2OE	7	I	Output Enable for buffer 2
1Y	6	O	Output
2Y	3	O	Output
GND	4	—	Ground
V _{CC}	8	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

 See⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range ⁽²⁾		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		-65	150	°C
T_J	Junction temperature			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4	mA
		V _{CC} = 2.3 V		–8	
		V _{CC} = 3 V		–16	
				–24	
		V _{CC} = 4.5 V		–32	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
				24	
		V _{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature	–40	125	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DCT	DCU	YZP	UNIT
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –4 mA	1.65 V	1.2			1.2			
	I _{OH} = –8 mA	1.8 V	1.4						
		2.3 V	1.9			1.9			
	I _{OH} = –16 mA	3 V	2.4			2.4			
	I _{OH} = –24 mA		2.3			2.3			
I _{OH} = –32 mA	4.5 V	3.8			3.8				
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V				0.1			V
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	1.8 V				0.45			
		2.3 V				0.3			
	I _{OL} = 16 mA	3 V				0.4			
	I _{OL} = 24 mA					0.55			
I _{OL} = 32 mA	4.5 V				0.55				
I _I	A or $\overline{\text{OE}}$ inputs	V _I = 5.5 V or GND	0 to 5.5 V						μA
I _{off}		V _I or V _O = 5.5 V	0			±10			μA
I _{OZ}		V _O = 0 to 5.5 V	3.6 V			10			μA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10			μA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500			μA
C _i	Data inputs	V _I = V _{CC} or GND	3.3 V			3.5			pF
	Control inputs					4			
C _o		V _O = V _{CC} or GND	3.3 V			6.5			pF

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	3.3	9.1	1.5	4.8	1.4	4.3	1	3.7	ns
t _{en}	$\overline{\text{OE}}$	Y	4	9.9	1.9	5.6	1.2	4.7	1.2	3.8	ns
t _{dis}	$\overline{\text{OE}}$	Y	1.5	11.6	1	5.8	1.4	4.6	1	3.4	ns

6.7 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

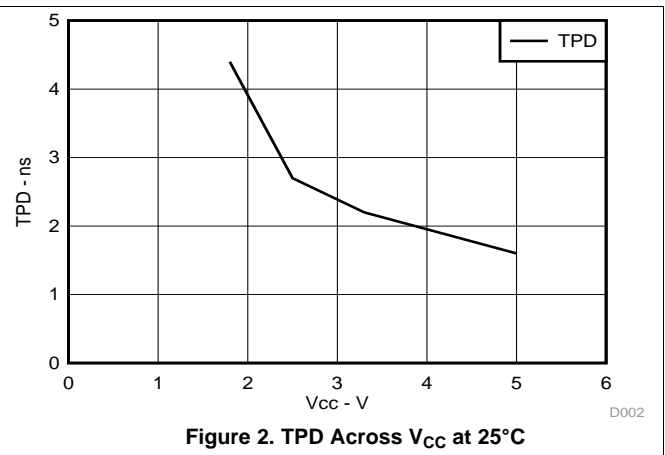
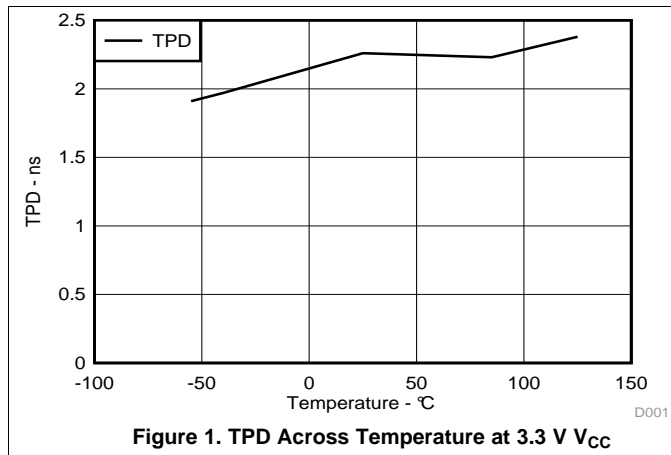
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	3.3	10.1	1.5	5.8	1.4	5.3	1	4.2	ns
t _{en}	$\overline{\text{OE}}$	Y	4	10.9	1.9	6.6	1.2	5.7	1.2	4.3	ns
t _{dis}	$\overline{\text{OE}}$	Y	1.5	12.6	1	6.8	1.4	5.6	1	3.9	ns

6.8 Operating Characteristics

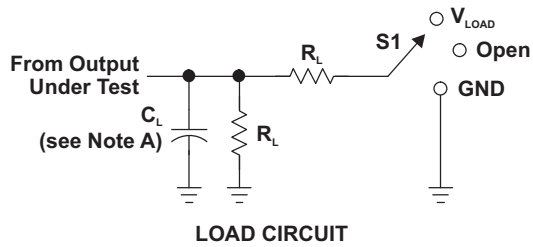
T_A = 25°

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT	
			TYP	TYP	TYP	TYP		
C _{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	19	19	20	22	pF
		Outputs disabled		2	2	2	3	

6.9 Typical Characteristics

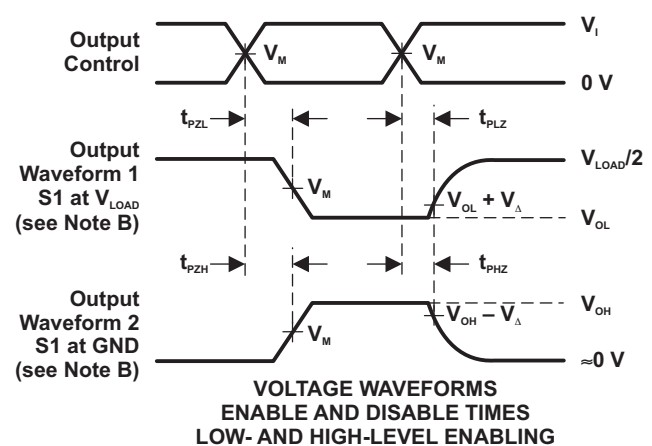
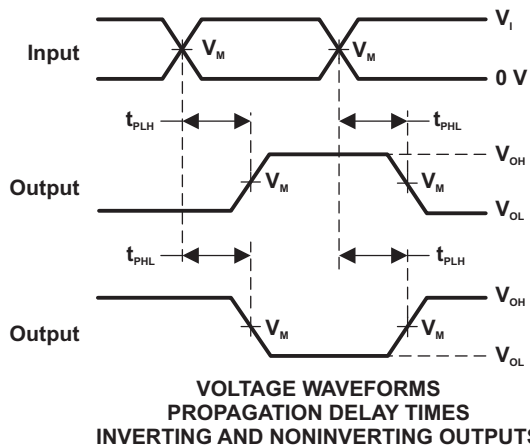
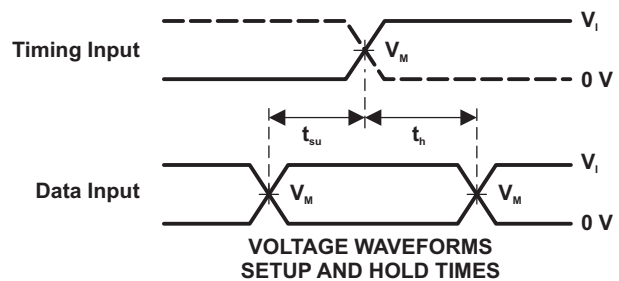
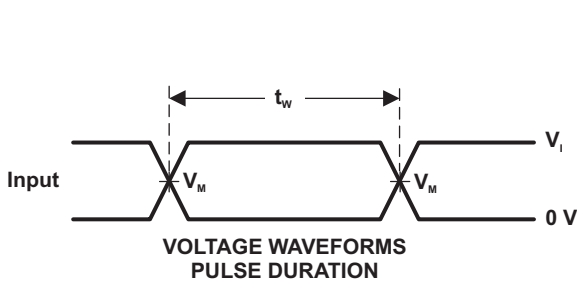


7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_i	t_i/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

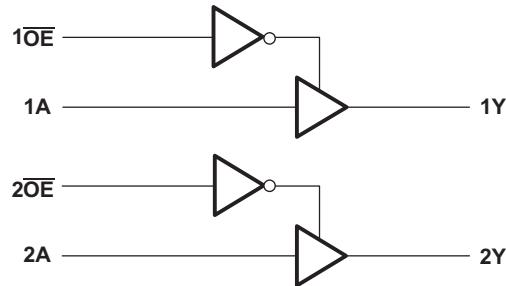
Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC2G125 device contains dual buffer gate device with output enable control and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 5.5 V
- Allows down voltage translation
- Inputs accept voltages to 5.5 V
- I_{off} Feature
 - Allows voltages on the inputs and outputs, when V_{CC} is 0 V

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G125 device is a high drive CMOS device that can be used as a output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC} .

9.2 Typical Application

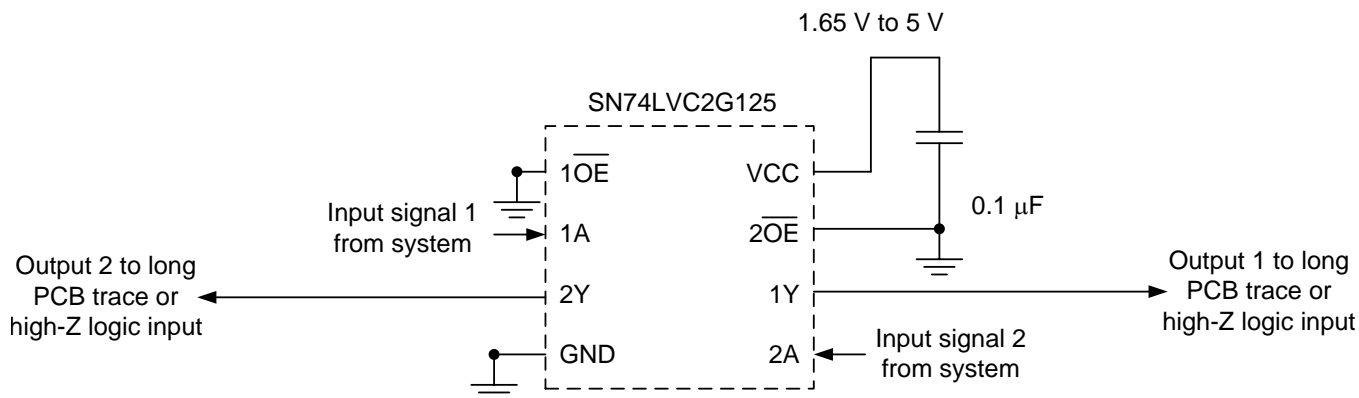


Figure 4. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:

- For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
- For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [Recommended Operating Conditions](#) table at any valid V_{CC} .

2. Recommend Output Conditions:

- Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above V_{CC} .

Typical Application (continued)

9.2.3 Application Curves

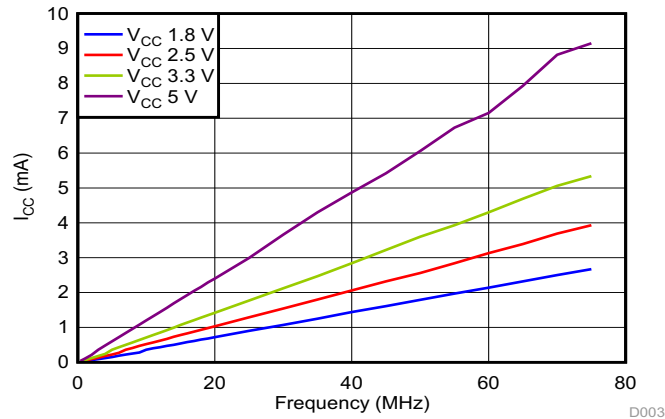


Figure 5. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-μF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

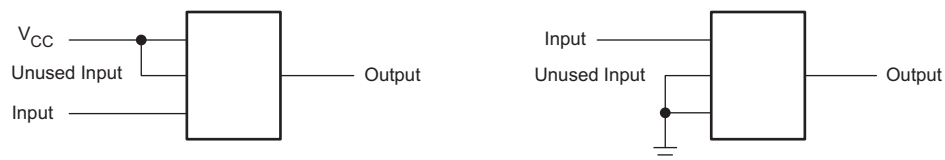


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC2G125DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C25 Z	Samples
74LVC2G125DCTRE6	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-40 to 125	C25 Z	Samples
74LVC2G125DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C25 Z	Samples
74LVC2G125DCURE4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C25R	Samples
74LVC2G125DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C25R	Samples
74LVC2G125DCUTE4	ACTIVE	VSSOP	DCU	8		TBD	Call TI	Call TI	-40 to 125		Samples
74LVC2G125DCUTG4	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C25R	Samples
SN74LVC2G125DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C25 Z	Samples
SN74LVC2G125DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(25 ~ C25Q ~ C25R) CZ	Samples
SN74LVC2G125DCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(C25Q ~ C25R)	Samples
SN74LVC2G125YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(CM7 ~ CMN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2G125 :

- Automotive: [SN74LVC2G125-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2G125DCTRE6	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
74LVC2G125DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
74LVC2G125DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G125DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G125DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74LVC2G125YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

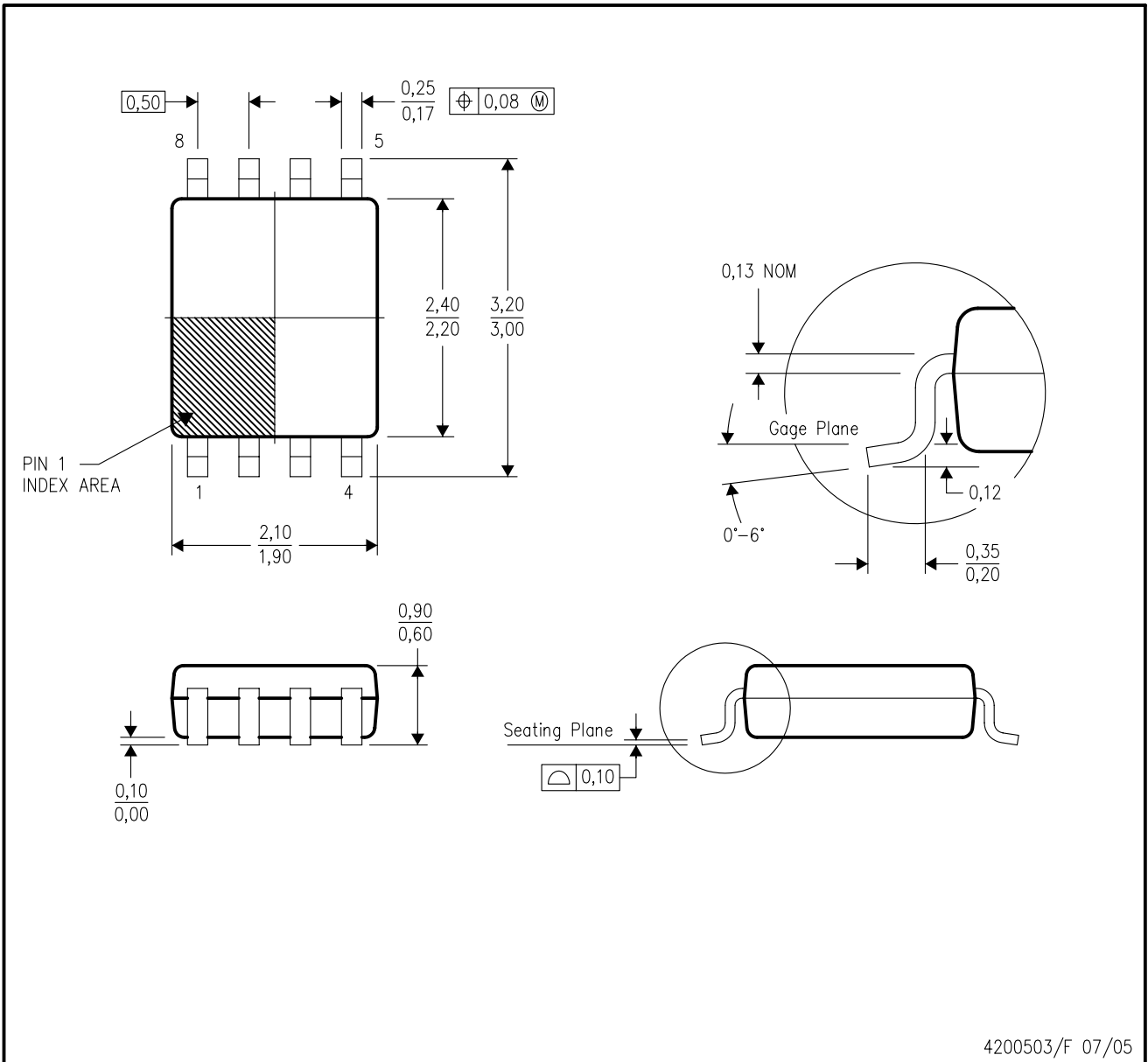
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2G125DCTRE6	SM8	DCT	8	3000	182.0	182.0	20.0
74LVC2G125DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
74LVC2G125DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G125DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G125DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74LVC2G125YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCU (R-PDSO-G8)

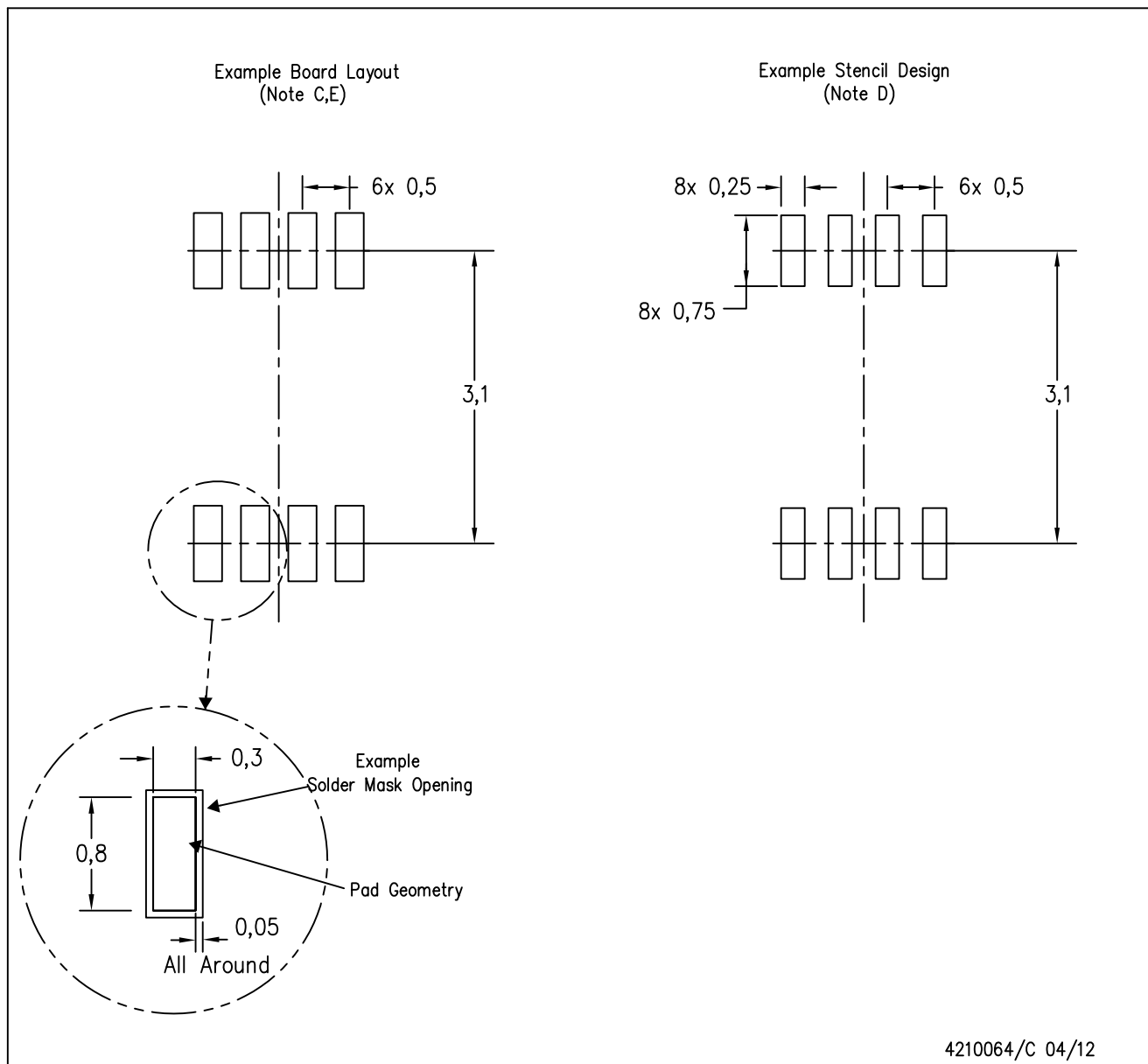
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

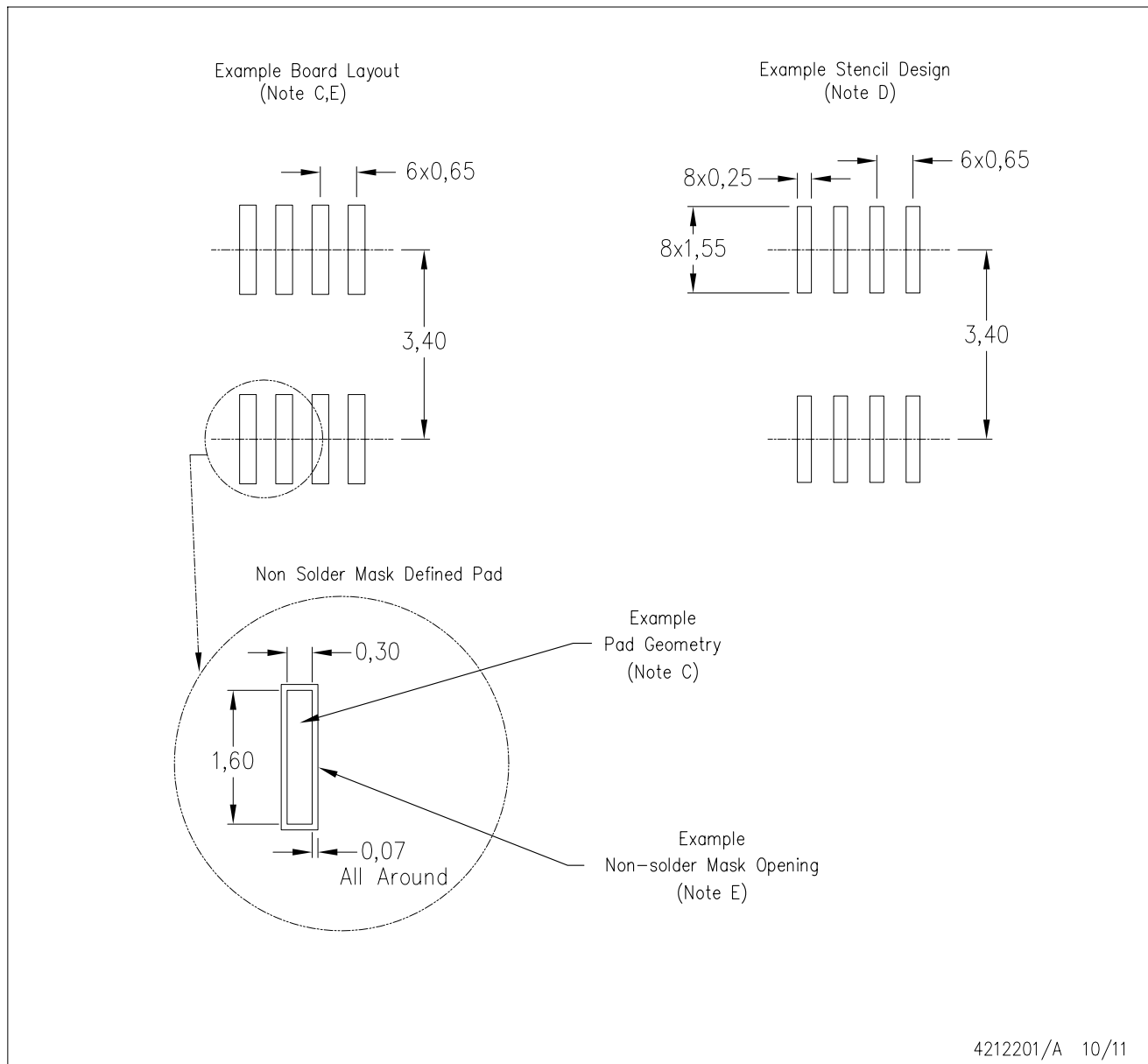


4188781/C 09/02

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion
 - D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

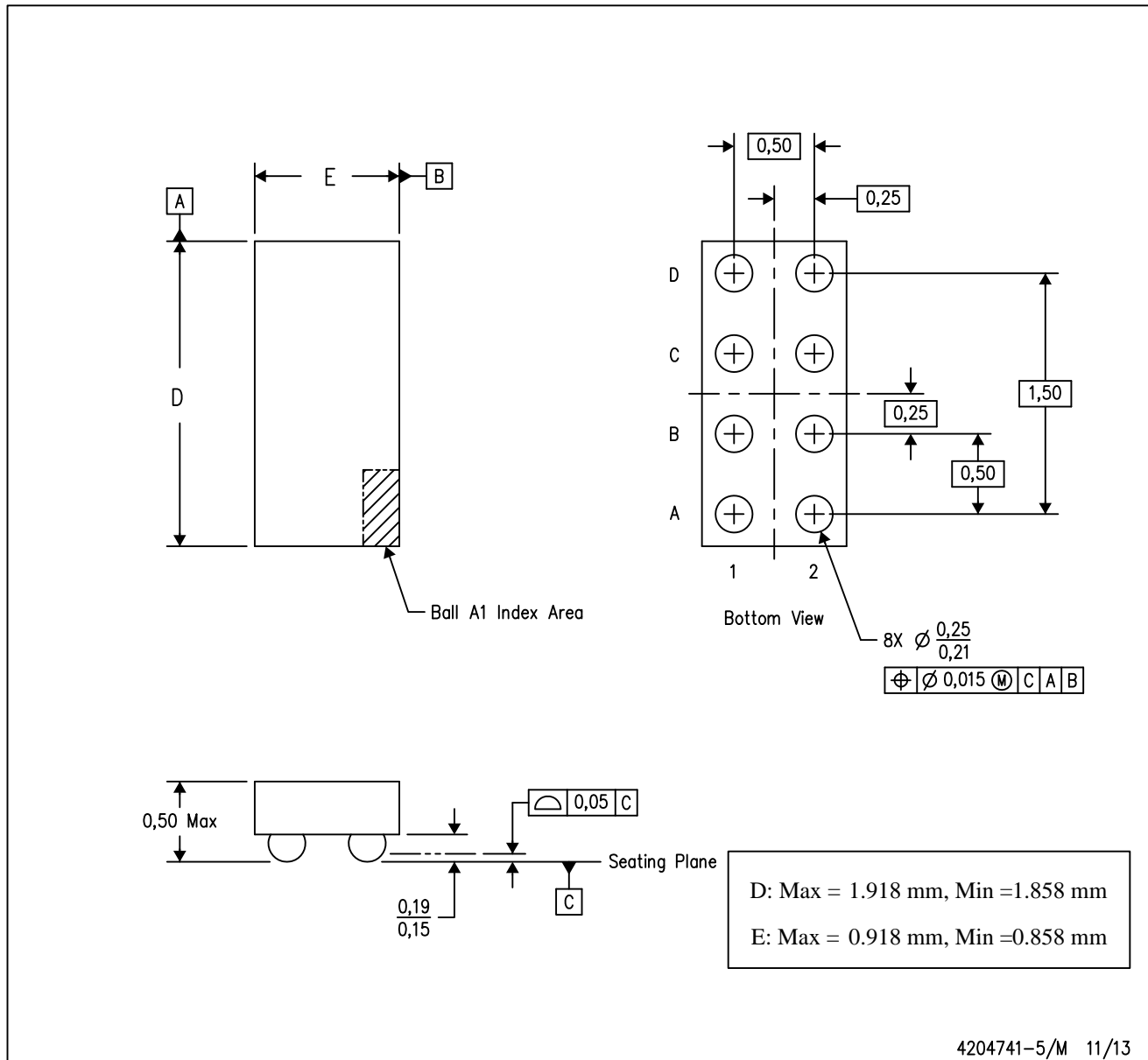
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated