

SN74LVC2T45 Dual-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Max Data Rates
 - 420 Mbps (3.3-V to 5-V Translation)
 - 210 Mbps (Translate to 3.3 V)
 - 140 Mbps (Translate to 2.5 V)
 - 75 Mbps (Translate to 1.8 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 4000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Personal Electronic
- Industrial
- Enterprise
- Telecom

3 Description

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

The SN74LVC2T45 is designed so that the DIR input circuit is supplied by V_{CCA} . This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state. NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2T45	SSOP (8)	2.95 mm x 2.80 mm
	VSSOP (8)	2.30 mm x 2.00 mm
	DSBGA (8)	1.89 mm x 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram

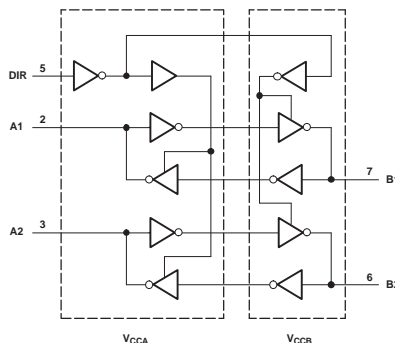


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4 Revision History

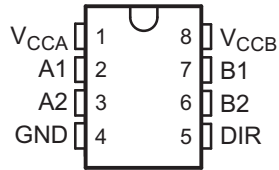
Changes from Revision I (March 2007) to Revision J

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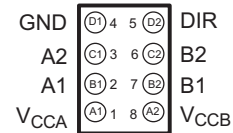
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1
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5 Pin Configuration and Functions

DCT or DCU Package
8-Pin SM8 or US8
Top View



YZP Package
8-Pin DSGBA
Bottom View



Pin Functions

NO.	PIN	TYPE	DESCRIPTION
	NAME		
1	V _{CCA}	P	A-port supply voltage. $1.65\text{ V} \leq V_{CCA} \leq 5.5\text{ V}$
2	A1	I/O	Input/output A1. Referenced to V _{CCA}
3	A2	I/O	Input/output A2. Referenced to V _{CCA}
4	GND	G	Ground
5	DIR	I	Direction control signal
6	B2	I/O	Input/output B2. Referenced to V _{CCB}
7	B1	I/O	Input/output B1. Referenced to V _{CCB}
8	V _{CCB}	P	B-port supply voltage. $1.65\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$

Pin Functions

PIN			TYPE	DESCRIPTION
BALL	NAME	NO.		
A1	V _{CCA}	1	P	A-port supply voltage. $1.65\text{ V} \leq V_{CCA} \leq 5.5\text{ V}$
A2	V _{CCB}	8	P	B-port supply voltage. $1.65\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$
B1	A1	2	I/O	Input/output A1. Referenced to V _{CCA}
B2	B1	7	I/O	Input/output B1. Referenced to V _{CCB}
C1	A2	3	I/O	Input/output A2. Referenced to V _{CCA}
C2	B2	6	I/O	Input/output B2. Referenced to V _{CCB}
D1	GND	4	G	Ground
D2	DIR	5	I	Direction control signal

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CCA}	Supply voltage range	-0.5	6.5	V
V_{CCB}				
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ^{(2) (3)}	A port	$V_{CCA} + 0.5$	V
		B port	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		±50	mA
T_{stg}	Storage temperature range	-65	150	°C
	Continuous current through V_{CC} or GND		±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine model (A115-A)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

		V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.65	5.5	V
V_{CCB}				1.65	5.5	
V_{IH}	High-level input voltage	Data inputs ⁽⁴⁾	1.65 V to 1.95 V	$V_{CCI} \times 0.65$		V
			2.3 V to 2.7 V	1.7		
			3 V to 3.6 V	2		
			4.5 V to 5.5 V	$V_{CCI} \times 0.7$		
V_{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.65 V to 1.95 V	$V_{CCI} \times 0.35$		V
			2.3 V to 2.7 V	0.7		
			3 V to 3.6 V	0.8		
			4.5 V to 5.5 V	$V_{CCI} \times 0.3$		

- (1) V_{CCI} is the V_{CC} associated with the input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (4) For V_{CCI} values not specified in the data sheet, $V_{IH \text{ min}} = V_{CCI} \times 0.7 \text{ V}$, $V_{IL \text{ max}} = V_{CCI} \times 0.3 \text{ V}$.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{IH}	High-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.65 V to 1.95 V		V _{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V _{CCA} × 0.7		
V _{IL}	Low-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.65 V to 1.95 V			V _{CCA} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V _{CCA} × 0.3	
V _I	Input voltage			0	5.5	V	
V _O	Output voltage			0	V _{CCO}	V	
I _{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I _{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
Δt/Δv	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
		Control input	1.65 V to 5.5 V			5	
T _A	Operating free-air temperature			–40	85	°C	

(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC2T45			UNIT
		DCT	DCU	YZP	
		8 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	184.0	203.6	105.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	114.7	75.9	1.6	
R _{θJB}	Junction-to-board thermal resistance	96.4	82.3	10.8	
ψ _{JT}	Junction-to-top characterization parameter	40.8	7.2	3.1	
ψ _{JB}	Junction-to-board characterization parameter	95.4	81.9	10.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics⁽¹⁾⁽²⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CCA}	V _{CCB}	T _A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V _{OH}		V _I = V _{IH}	1.65 V to 4.5 V	1.65 V to 4.5 V				V _{CCO} – 0.1		V
			1.65 V	1.65 V				1.2		
			2.3 V	2.3 V				1.9		
			3 V	3 V				2.4		
			4.5 V	4.5 V				3.8		
V _{OL}		V _I = V _{IL}	1.65 V to 4.5 V	1.65 V to 4.5 V				0.1		V
			1.65 V	1.65 V				0.45		
			2.3 V	2.3 V				0.3		
			3 V	3 V				0.55		
			4.5 V	4.5 V				0.55		
I _I	DIR	V _I = V _{CCA} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V				±1	±2	µA
I _{off}	A port	V _I or V _O = 0 to 5.5 V	0 V	0 to 5.5 V				±1	±2	µA
	B port		0 to 5.5 V	0 V				±1	±2	
I _{OZ}	A or B port	V _O = V _{CCO} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V				±1	±2	µA
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					3	µA
			5 V	0 V					2	
			0 V	5 V					–2	
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					3	µA
			5 V	0 V					–2	
			0 V	5 V					2	
I _{CCA} + I _{CCB} (see Table 3)		V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					4	µA
ΔI _{CCA}	A port	One A port at V _{CCA} – 0.6 V, DIR at V _{CCA} , B port = open	3 V to 5.5 V	3 V to 5.5 V					50	µA
	DIR				DIR at V _{CCA} – 0.6 V, B port = open, A port at V _{CCA} or GND					
ΔI _{CCB}	B port	One B port at V _{CCB} – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V					50	µA
C _I	DIR	V _I = V _{CCA} or GND	3.3 V	3.3 V			2.5			pF
C _{io}	A or B port	V _O = V _{CCA/B} or GND	3.3 V	3.3 V			6			pF

 (1) V_{CCO} is the V_{CC} associated with the output port.

 (2) V_{CCI} is the V_{CC} associated with the input port.

6.6 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

 over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 17)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		V _{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	3	17.7	2.2	10.3	1.7	8.3	1.4	7.2	ns
t _{PHL}			2.8	14.3	2.2	8.5	1.8	7.1	1.7	7	
t _{PLH}	B	A	3	17.7	2.3	16	2.1	15.5	1.9	15.1	ns
t _{PHL}			2.8	14.3	2.1	12.9	2	12.6	1.8	12.2	
t _{PHZ}	DIR	A	10.6	30.9	10.3	30.5	10.5	30.5	10.7	29.3	ns
t _{PLZ}			7.3	19.7	7.5	19.6	7.5	19.5	7	19.4	

Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (continued)

 over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see [Figure 17](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHZ}	DIR	B	10	27.9	8.4	14.9	6.5	11.3	4.1	8.6	ns
t_{PLZ}			6.5	19.5	7.2	12.6	4.3	9.7	2.1	7.1	
$t_{PZH}^{(1)}$	DIR	A	37.2		28.6		25.2		22.2		ns
$t_{PZL}^{(1)}$			42.2		27.8		23.9		20.8		
$t_{PZH}^{(1)}$	DIR	B	37.4		29.9		27.8		26.6		ns
$t_{PZL}^{(1)}$			45.2		39		37.6		36.3		

 (1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

6.7 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

 over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 17](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	16	1.5	8.5	1.3	6.4	1.1	5.1	ns
t_{PHL}			2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	
t_{PLH}	B	A	2.2	10.3	1.5	8.5	1.4	8	1	7.5	ns
t_{PHL}			2.2	8.5	1.4	7.5	1.3	7	0.9	6.2	
t_{PHZ}	DIR	A	6.6	17.1	7.1	16.8	6.8	16.8	5.2	16.5	ns
t_{PLZ}			5.3	12.6	5.2	12.5	4.9	12.3	4.8	12.3	
t_{PHZ}	DIR	B	10.7	27.9	8.1	13.9	5.8	10.5	3.5	7.6	ns
t_{PLZ}			7.8	18.9	6.2	11.2	3.6	8.9	1.4	6.2	
$t_{PZH}^{(1)}$	DIR	A	29.2		19.7		16.9		13.7		ns
$t_{PZL}^{(1)}$			36.4		21.4		17.5		13.8		
$t_{PZH}^{(1)}$	DIR	B	28.6		21		18.7		17.4		ns
$t_{PZL}^{(1)}$			30		24.3		22.2		21.1		

 (1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

6.8 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

 over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Figure 17](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	15.5	1.4	8	0.7	5.6	0.7	4.4	ns
t_{PHL}			2	12.6	1.3	7	0.8	5	0.7	4	
t_{PLH}	B	A	1.7	8.3	1.3	6.4	0.7	5.8	0.6	5.4	ns
t_{PHL}			1.8	7.1	1.3	5.4	0.8	5	0.7	4.5	
t_{PHZ}	DIR	A	5	10.9	5.1	10.8	5	10.8	5	10.4	ns
t_{PLZ}			3.4	8.4	3.7	8.4	3.9	8.1	3.3	7.8	
t_{PHZ}	DIR	B	11.2	27.3	8	13.7	5.8	10.4	2.9	7.4	ns
t_{PLZ}			9.4	17.7	5.6	11.3	4.3	8.3	1	5.6	
$t_{PZH}^{(1)}$	DIR	A	26		17.7		14.1		11		ns
$t_{PZL}^{(1)}$			34.4		19.1		15.4		11.9		

 (1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics: $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (continued)

 over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 17](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PZH}^{(1)}$	DIR	B	23.9		16.4		13.9		12.2		ns
$t_{PZL}^{(1)}$			23.5		17.8		15.8		14.4		

6.9 Switching Characteristics: $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$

 over recommended operating free-air temperature range, $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 17](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	15.1	1	7.5	0.6	5.4	0.5	3.9	ns
t_{PHL}			1.8	12.2	0.9	6.2	0.7	4.5	0.5	3.5	
t_{PLH}	B	A	1.4	7.2	1	5.1	0.7	4.4	0.5	3.9	ns
t_{PHL}			1.7	7	0.9	4.6	0.7	4	0.5	3.5	
t_{PHZ}	DIR	A	2.9	8.2	2.9	7.9	2.8	7.9	2.2	7.8	ns
t_{PLZ}			1.4	6.9	1.3	6.7	0.7	6.7	0.7	6.6	
t_{PHZ}	DIR	B	11.2	26.1	7.2	13.9	5.8	10.1	1.3	7.3	ns
t_{PLZ}			8.4	16.9	5	11	4	7.7	1	5.6	
$t_{PZH}^{(1)}$	DIR	A	24.1		16.1		12.1		9.5		ns
$t_{PZL}^{(1)}$			33.1		18.5		14.1		10.8		
$t_{PZH}^{(1)}$	DIR	B	22		14.2		12.1		10.5		ns
$t_{PZL}^{(1)}$			20.4		14.1		12.4		11.3		

 (1) The enable time is a calculated value, derived using the formula shown in the [Enable Times](#) section.

6.10 Operating Characteristics
 $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.8 \text{ V}$	$V_{CCA} = V_{CCB} = 2.5 \text{ V}$	$V_{CCA} = V_{CCB} = 3.3 \text{ V}$	$V_{CCA} = V_{CCB} = 5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A-port input, B-port output	3	4	4	4	pF
	B-port input, A-port output	18	19	20	21	
$C_{pdB}^{(1)}$	A-port input, B-port output	18	19	20	21	pF
	B-port input, A-port output	3	4	4	4	

(1) Power dissipation capacitance per transceiver

6.11 Typical Characteristics

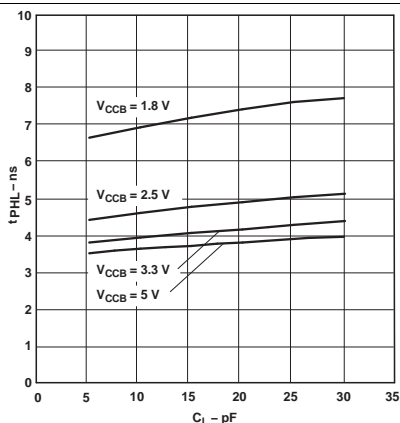


Figure 1. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

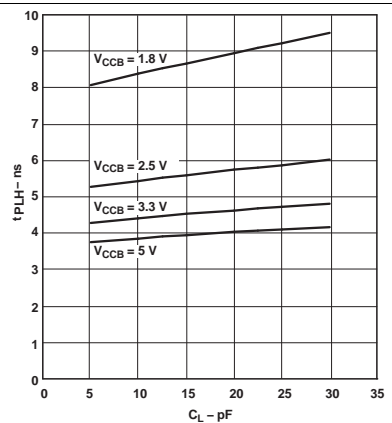


Figure 2. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

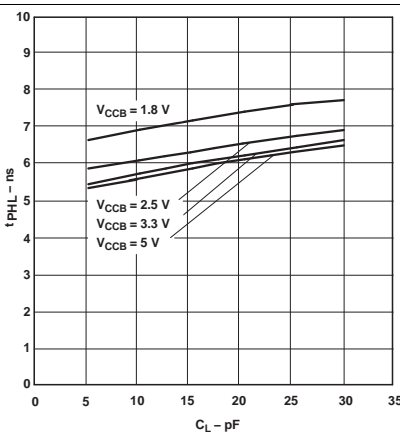


Figure 3. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

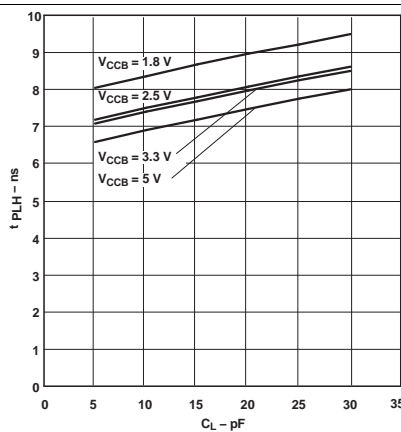


Figure 4. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

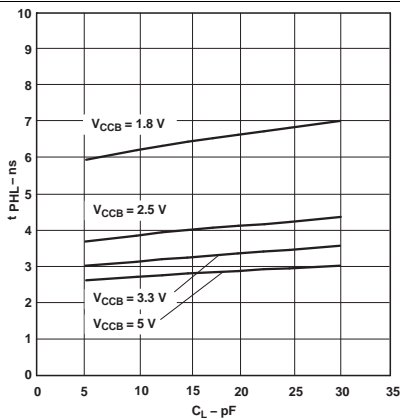


Figure 5. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

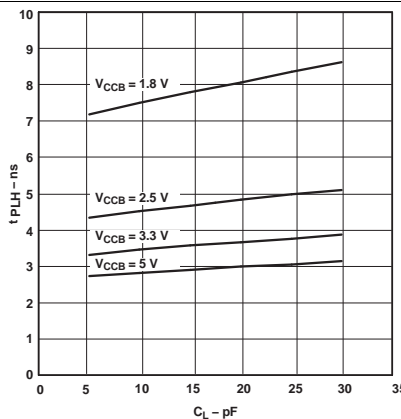


Figure 6. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

Typical Characteristics (continued)

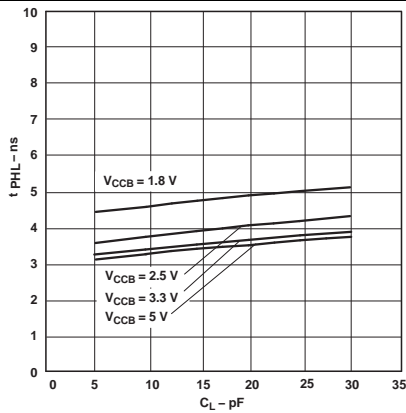


Figure 7. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

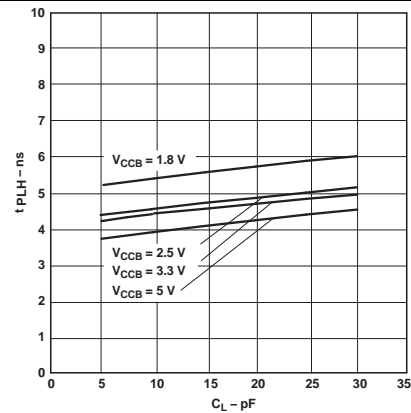


Figure 8. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

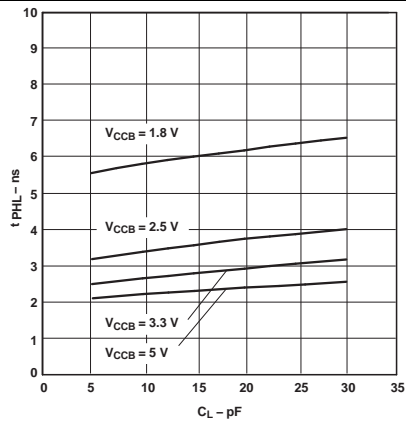


Figure 9. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

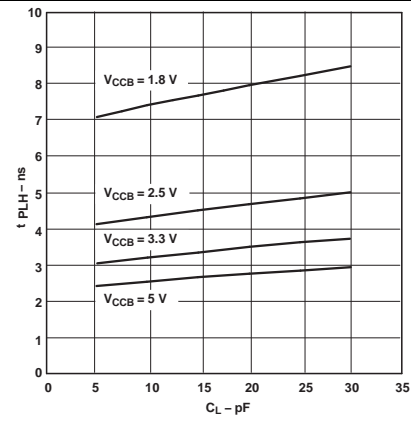


Figure 10. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

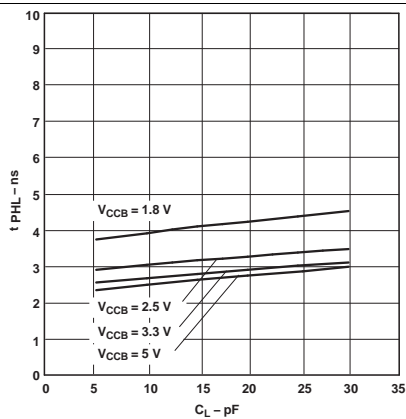


Figure 11. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

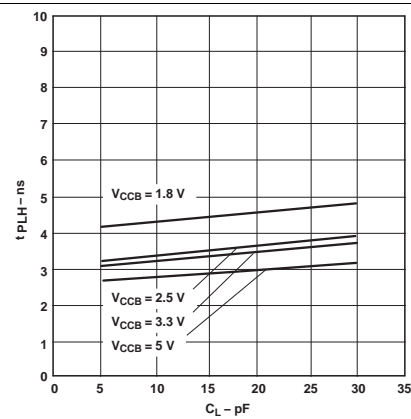


Figure 12. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

Typical Characteristics (continued)

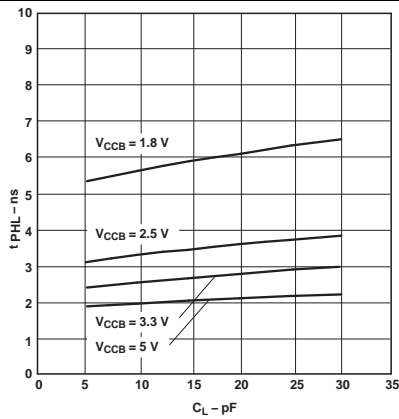


Figure 13. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

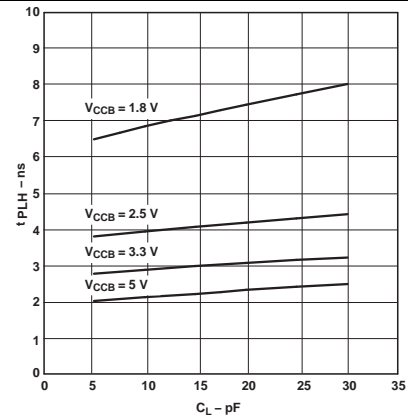


Figure 14. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

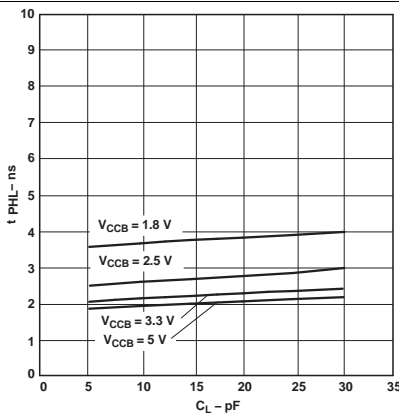


Figure 15. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

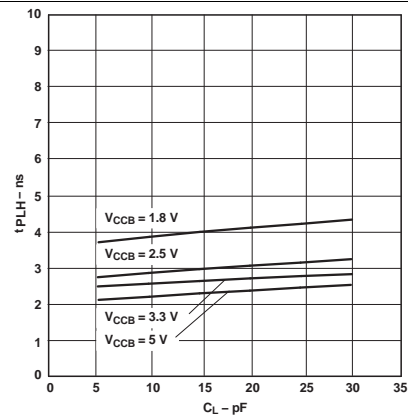
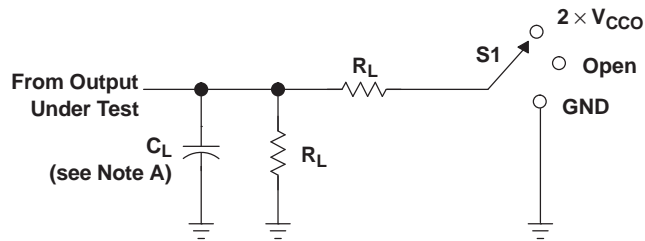


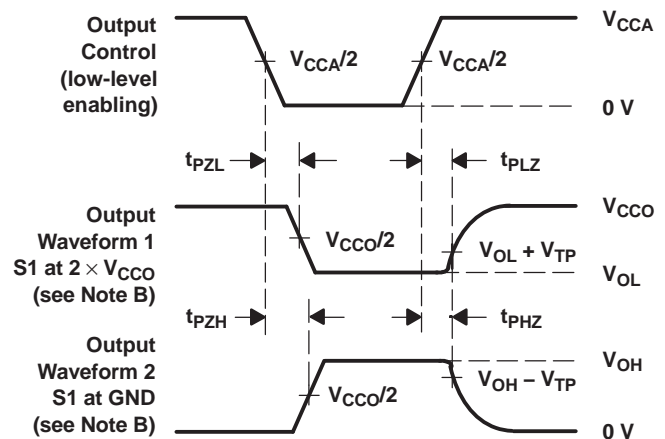
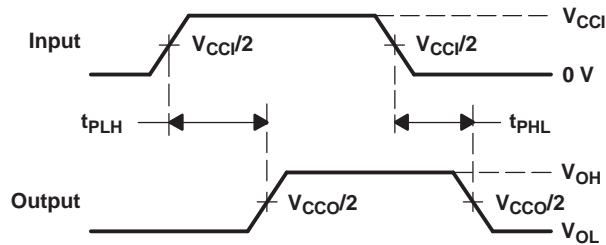
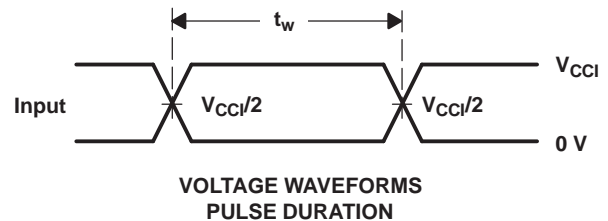
Figure 16. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

7 Parameter Measurement Information


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
$1.8 \text{ V} \pm 0.15 \text{ V}$	15 pF	2 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	15 pF	2 k Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	15 pF	2 k Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	15 pF	2 k Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $dv/dt \geq 1 \text{ V/ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCi} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.
 - All parameters and waveforms are not applicable to all devices.

Figure 17. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC2T45 is dual-bit, dual-supply noninverting voltage level translation. Pin Ax and direction control pin are support by V_{CCA} and pin Bx are support by V_{CCB} . The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A.

8.2 Functional Block Diagram

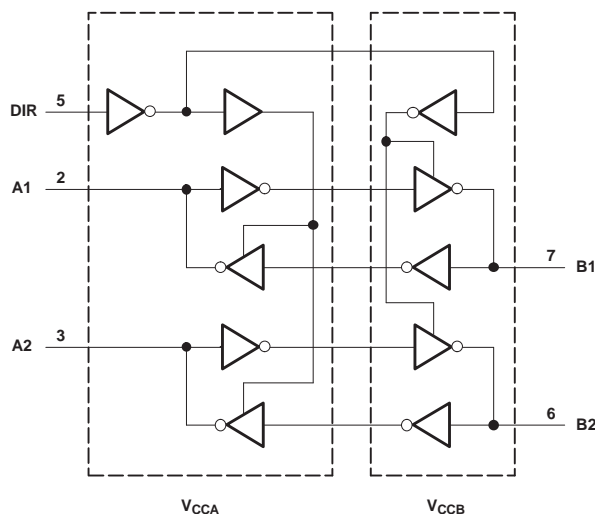


Figure 18. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65 V and 5.5 V making the device suitable for translating between any of the voltage nodes (1.8-V, 2.5-V, 3.3-V and 5-V).

8.3.2 Support High-Speed Translation

SN74LVC2T45 can support high data rate application. The translated signal data rate can be up to 420 Mbps when signal is translated from 3.3 V to 5 V.

8.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

8.4 Device Functional Modes

Table 1. Function Table⁽¹⁾ (Each Transceiver)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

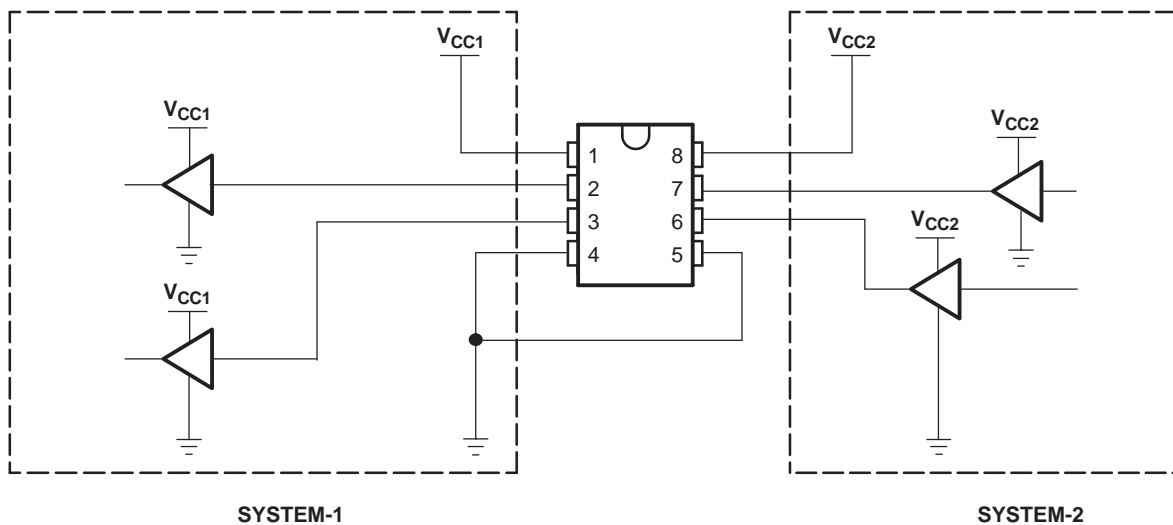
9.1 Application Information

The SN74LVC2T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The max data rate can be up to 420 Mbps when device translate signal from 3.3 V to 5 V.

9.2 Typical Applications

9.2.1 Unidirectional Logic Level-Shifting Application

The following shows an example of the SN74LVC2T45 being used in a unidirectional logic level-shifting application.



PIN	NAME	FUNCTION	DESCRIPTION
1	V _{CCA}	V _{CC1}	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
2	A1	OUT1	Output level depends on V _{CC1} voltage.
3	A2	OUT2	Output level depends on V _{CC1} voltage.
4	GND	GND	Device GND
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	B2	IN2	Input threshold value depends on V _{CC2} voltage.
7	B1	IN1	Input threshold value depends on V _{CC2} voltage.
8	V _{CCB}	V _{CC2}	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

Figure 19. Unidirectional Logic Level-Shifting Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#).

Table 2. Design Parameters

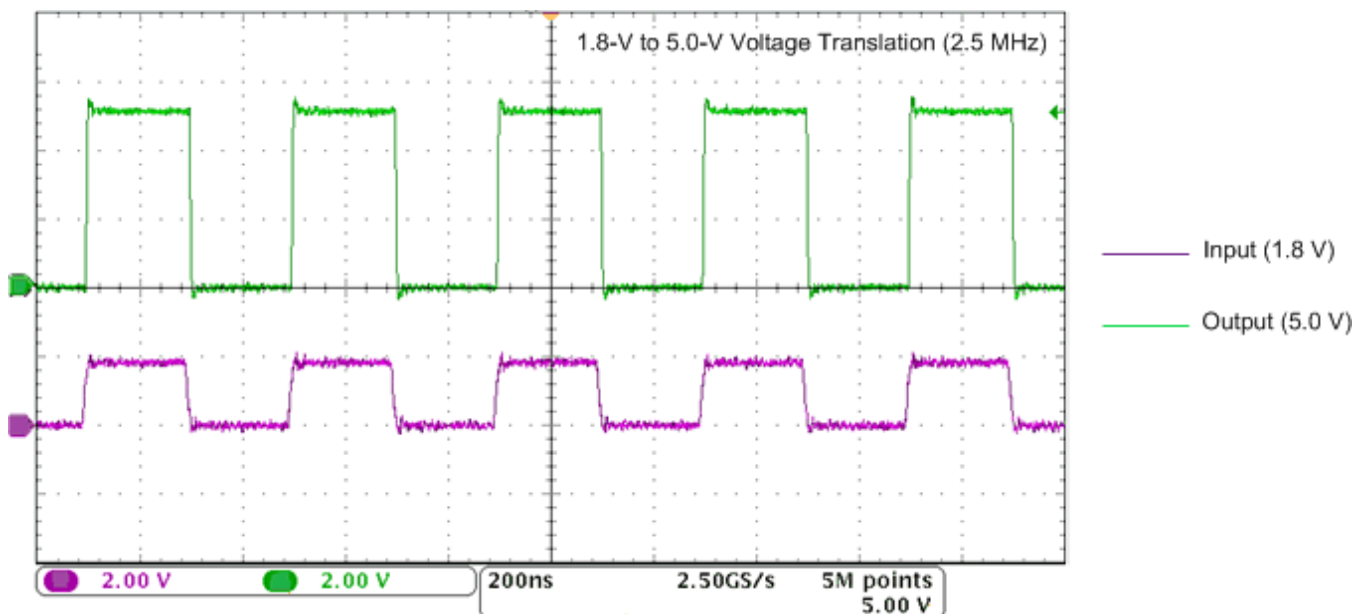
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 V to 5.5 V
Output voltage range	1.65 V to 5.5 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

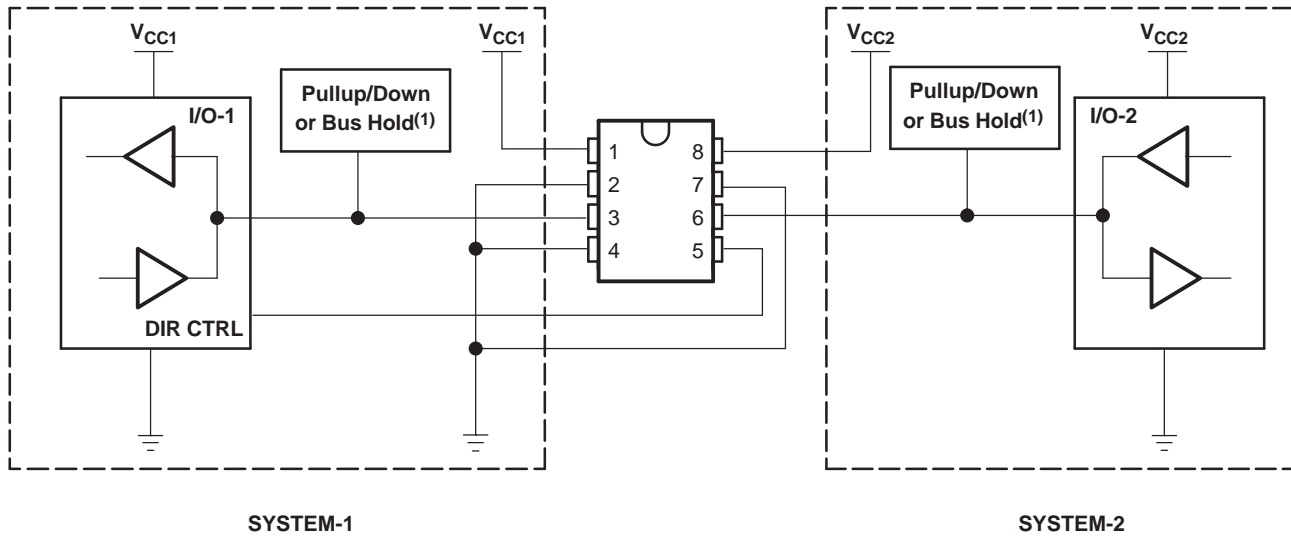
- Input voltage range
 - Use the supply voltage of the device that is driving the SN74LVC2T45 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74LVC2T45 device is driving to determine the output voltage range.

9.2.1.3 Application Curve



9.2.2 Bidirectional Logic Level-Shifting Application

Figure 20 shows the SN74LVC2T45 being used in a bidirectional logic level-shifting application. Because the SN74LVC2T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 20. Bidirectional Logic Level-Shifting Application

9.2.2.1 Design Requirements

Please refer to [Unidirectional Logic Level-Shifting Application](#).

9.2.2.2 Detailed Design Procedure

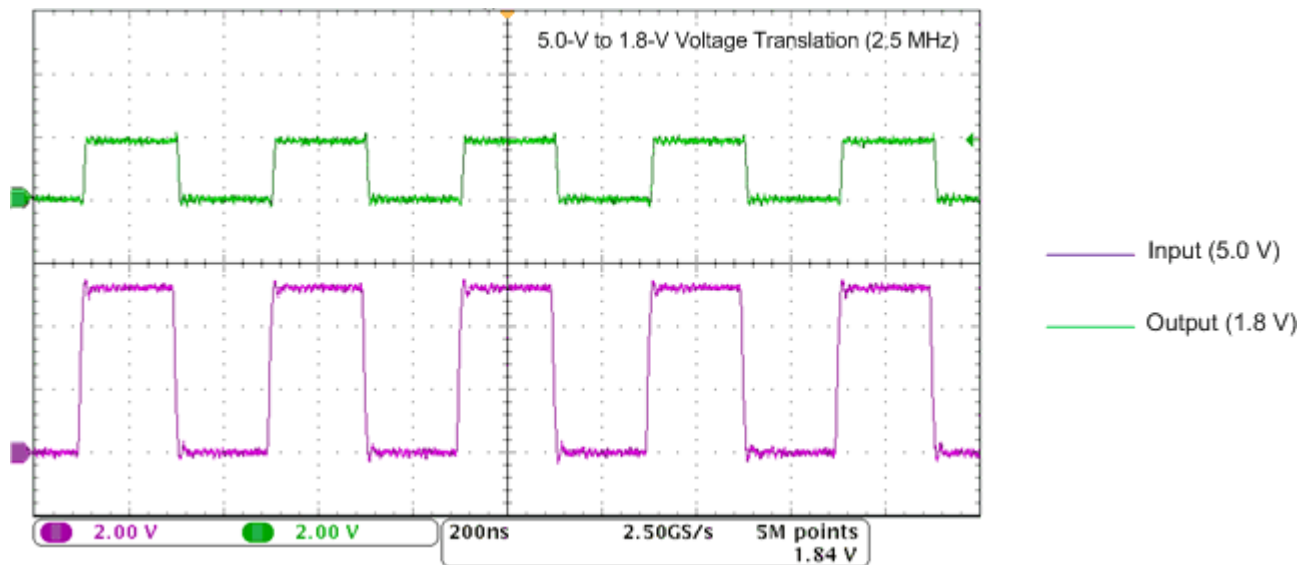
9.2.2.2.1 Enable Times

Calculate the enable times for the SN74LVC2T45 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

9.2.2.3 Application Curve



10 Power Supply Recommendations

10.1 Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA} .
3. V_{CCB} can be ramped up along with or after V_{CCA} .

Table 3. Typical Total Static Power Consumption ($I_{CCA} + I_{CCB}$)

V_{CCB}	V_{CCA}					UNIT
	0 V	1.8 V	2.5 V	3.3 V	5 V	
0 V	0	<1	<1	<1	<1	μA
1.8 V	<1	<2	<2	<2	2	
2.5 V	<1	<2	<2	<2	<2	
3.3 V	<1	<2	<2	<2	<2	
5 V	<1	2	<2	<2	<2	

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

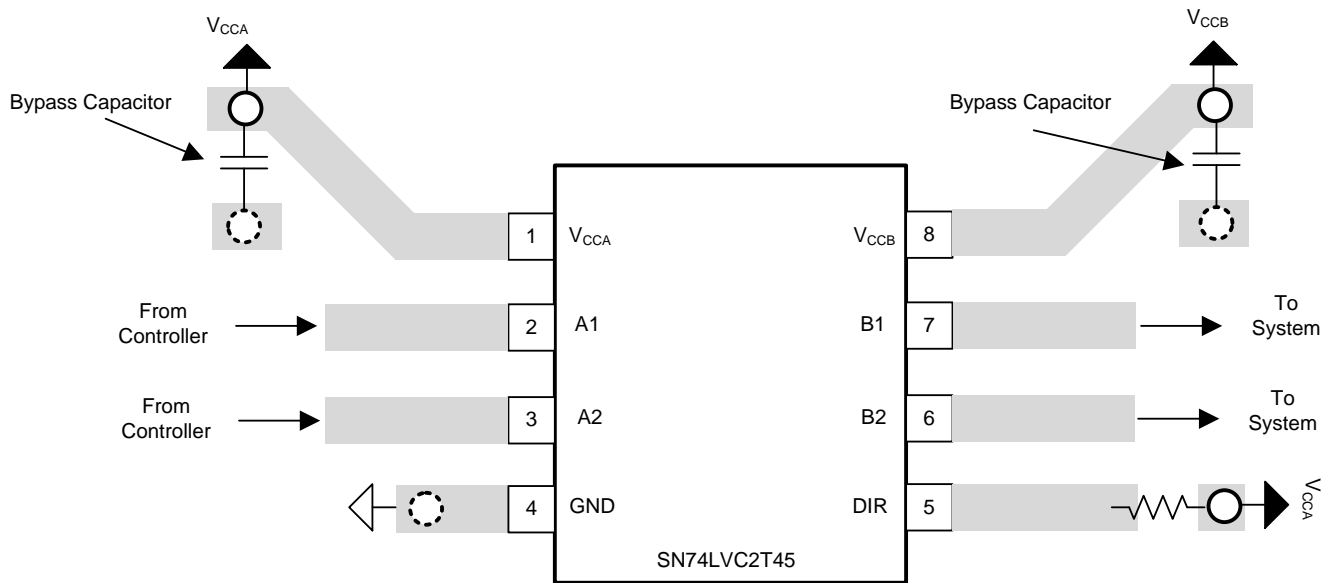
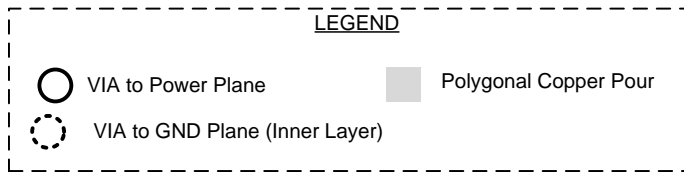
- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

SN74LVC2T45

SCES516J – DECEMBER 2003 – REVISED DECEMBER 2014

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11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2T45DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2 Z	Samples
SN74LVC2T45DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2 Z	Samples
SN74LVC2T45DCTT	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2 Z	Samples
SN74LVC2T45DCTTG4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2 Z	Samples
SN74LVC2T45DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(CT2Q ~ CT2R ~ T2) CZ	Samples
SN74LVC2T45DCURE4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R	Samples
SN74LVC2T45DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R	Samples
SN74LVC2T45DCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT2Q ~ CT2R ~ T2) CZ	Samples
SN74LVC2T45DCUTE4	ACTIVE	VSSOP	DCU	8		TBD	Call TI	Call TI	-40 to 85		Samples
SN74LVC2T45DCUTG4	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R	Samples
SN74LVC2T45YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TB ~ TB7 ~ TBN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC2T45 :

- Automotive: [SN74LVC2T45-Q1](#)
- Enhanced Product: [SN74LVC2T45-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2T45DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2T45DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2T45DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74LVC2T45DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2T45DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2T45YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1
SN74LVC2T45YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	2.0	8.0	Q1

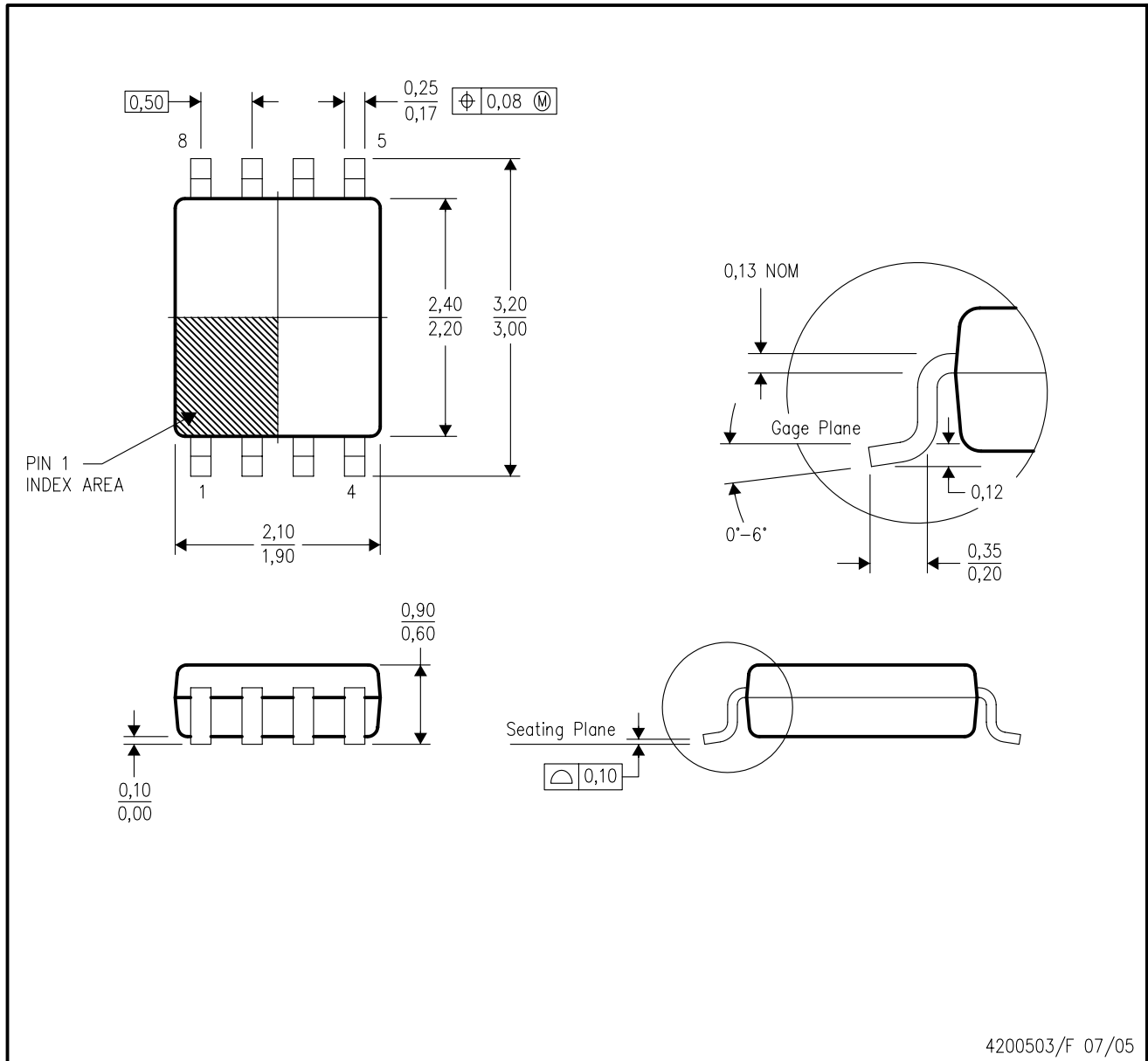
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2T45DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2T45DCTT	SM8	DCT	8	250	182.0	182.0	20.0
SN74LVC2T45DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74LVC2T45DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2T45DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2T45YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0
SN74LVC2T45YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4188781/C 09/02

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

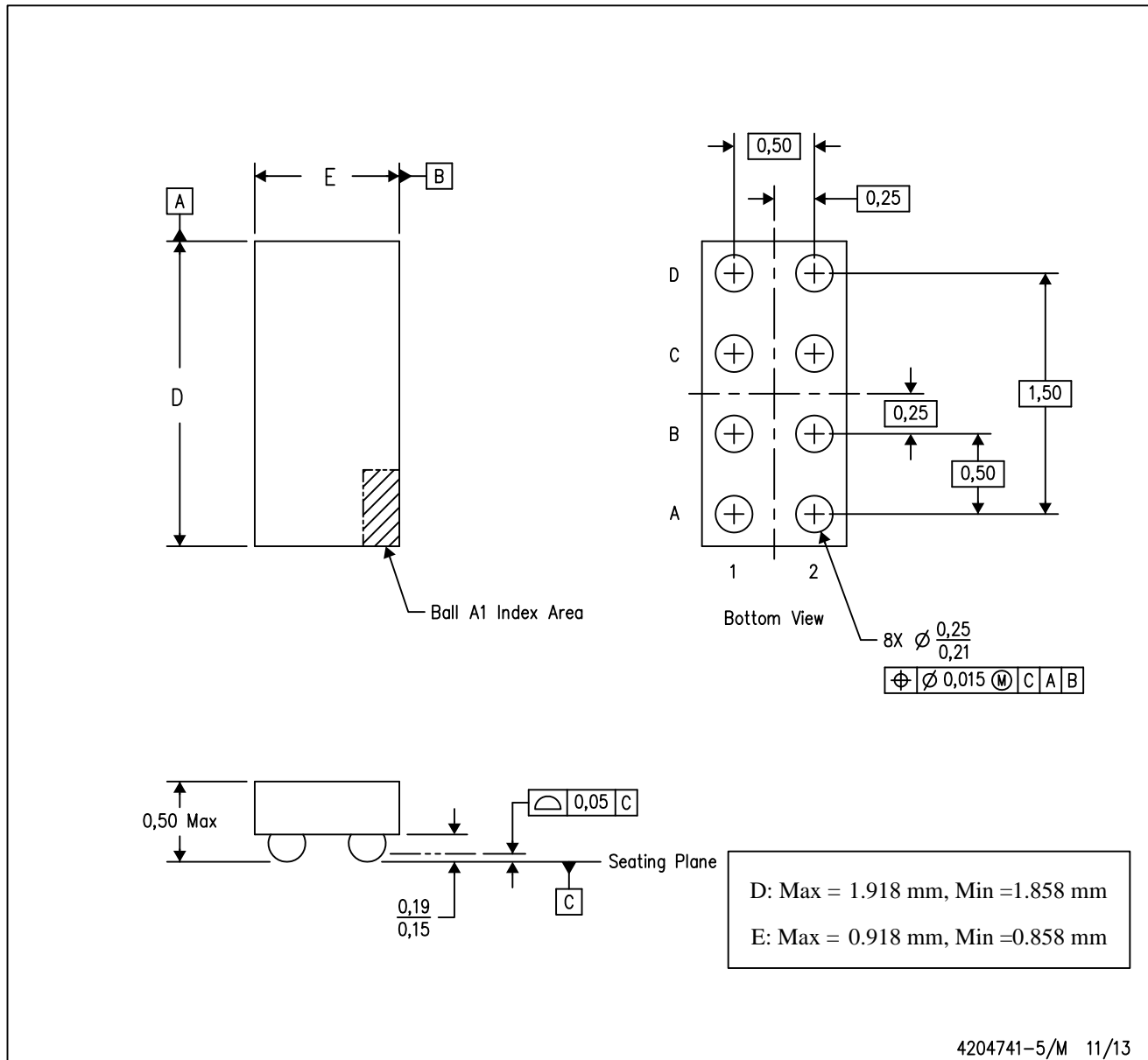
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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