

SN74LVC8T245-EP 8-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and Tri-State Outputs

1 Features

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Are in the High-Impedance State
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 4000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C) Temperature Range ⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

3 Description

This 8-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74LVC8T245-EP is optimized to operate with V_{CCA} and V_{CCB} set at 1.65 V to 5.5 V. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5.5-V voltage nodes.

The SN74LVC8T245-EP is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable (\overline{OE}) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CC2} .

The SN74LVC8T245-EP is designed so that the control pins (DIR and \overline{OE}) are supplied by V_{CCA} .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC8T245-EP	TSSOP (24)	4.40 mm × 7.80 mm
	SOIC (24)	7.50 mm × 15.40 mm
	VQFN (24)	3.50 mm × 5.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(1) Additional temperature ranges are available – contact factory.

Logic Diagram (Positive Logic)

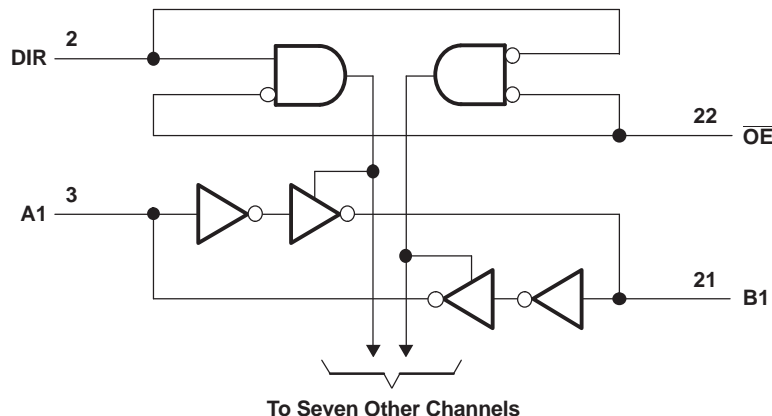


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2008) to Revision A	Page
• Added <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed <i>Ordering Information</i> table to <i>Device Information</i> table	1
• Added SOIC and VQFN packages to data sheet	1
• Added the temperature conditions for MIN, TYP, and MAX in the <i>Electrical Characteristics</i> table	6
• Changed $T_A = -55^{\circ}\text{C}$ to 125°C values for I_I , I_{off} , I_{OZ} , I_{CCA} , I_{CCB} , and $I_{\text{CCA}} + I_{\text{CCB}}$ in the <i>Electrical Characteristics</i> table	6

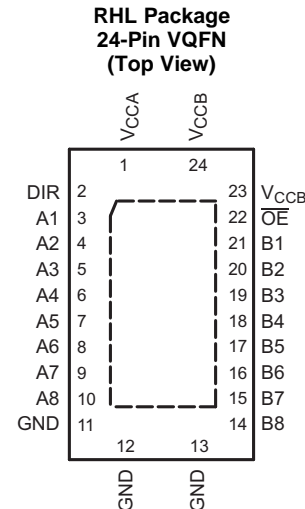
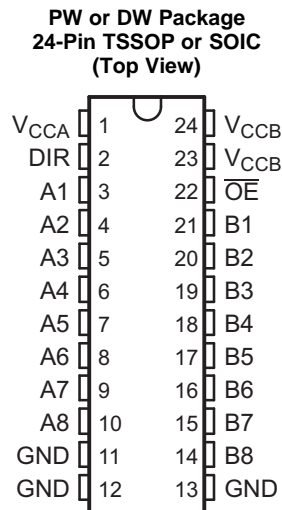
5 Description (continued)

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, all outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	3	I/O	Input/output A1. Referenced to V_{CCA} .
A2	4	I/O	Input/output A2. Referenced to V_{CCA} .
A3	5	I/O	Input/output A3. Referenced to V_{CCA} .
A4	6	I/O	Input/output A4. Referenced to V_{CCA} .
A5	7	I/O	Input/output A5. Referenced to V_{CCA} .
A6	8	I/O	Input/output A6. Referenced to V_{CCA} .
A7	9	I/O	Input/output A7. Referenced to V_{CCA} .
A8	10	I/O	Input/output A8. Referenced to V_{CCA} .
B1	21	I/O	Input/output B1. Referenced to V_{CCB} .
B2	20	I/O	Input/output B2. Referenced to V_{CCB} .
B3	19	I/O	Input/output B3. Referenced to V_{CCB} .
B4	18	I/O	Input/output B4. Referenced to V_{CCB} .
B5	17	I/O	Input/output B5. Referenced to V_{CCB} .
B6	16	I/O	Input/output B6. Referenced to V_{CCB} .
B7	15	I/O	Input/output B7. Referenced to V_{CCB} .
B8	14	I/O	Input/output B8. Referenced to V_{CCB} .
DIR	2	I	Direction-control signal.
GND	11, 12, 13	G	Ground.
\overline{OE}	22	I	Tri-state output-mode enables. Pull \overline{OE} high to place all outputs in tri-state mode. Referenced to V_{CCA} .
V_{CCA}	1	P	A-port supply voltage. $1.65\text{ V} \leq V_{CCA} \leq 5.5\text{ V}$.
V_{CCB}	23, 24	P	B-port supply voltage. $1.65\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V_{CCA} V_{CCB}	Supply voltage	-0.5	6.5	V	
V_I	Input voltage ⁽²⁾	I/O ports (A port)	-0.5	6.5	V
		I/O ports (B port)	-0.5	6.5	
		Control inputs	-0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A port	-0.5	6.5	V
		B port	-0.5	6.5	
V_O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$	-50	mA	
I_{OK}	Output clamp current	$V_O < 0$	-50	mA	
I_O	Continuous output current		±50	mA	
		Continuous current through each V_{CCA} , V_{CCB} , and GND	±100	mA	
$R_{\theta JA}$	Package thermal impedance ⁽⁴⁾		88	°C/W	
T_{stg}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5-V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine model	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.65	5.5	V
V _{CCB}					1.65	5.5	
V _{IH}	High-level input voltage	Data inputs ⁽⁵⁾	1.65 to 1.95 V		V _{CCI} × 0.65		V
			2.3 to 2.7 V		1.7		
			3 to 3.6 V		2		
			4.5 to 5.5 V		V _{CCI} × 0.7		
V _{IL}	Low-level input voltage	Data inputs ⁽⁵⁾	1.65 to 1.95 V		V _{CCI} × 0.35		V
			2.3 to 2.7 V		0.7		
			3 to 3.6 V		0.8		
			4.5 to 5.5 V		V _{CCI} × 0.3		
V _{IH}	High-level input voltage	Control inputs (referenced to V _{CCA}) ⁽⁶⁾	1.65 to 1.95 V		V _{CCA} × 0.65		V
			2.3 to 2.7 V		1.7		
			3 to 3.6 V		2		
			4.5 to 5.5 V		V _{CCA} × 0.7		
V _{IL}	Low-level input voltage	Control inputs (referenced to V _{CCA}) ⁽⁶⁾	1.65 to 1.95 V		V _{CCA} × 0.35		V
			2.3 to 2.7 V		0.7		
			3 to 3.6 V		0.8		
			4.5 to 5.5 V		V _{CCA} × 0.3		
V _I	Input voltage	Control inputs			0	5.5	V
V _{I/O}	Input/output voltage	Active state			0	V _{CCO}	V
		Tri-state			0	5.5	
I _{OH}	High-level output current		1.65 to 1.95 V		-4		mA
			2.3 to 2.7 V		-8		
			3 to 3.6 V		-24		
			4.5 to 5.5 V		-32		
I _{OL}	Low-level output current		1.65 to 1.95 V		4		mA
			2.3 to 2.7 V		8		
			3 to 3.6 V		24		
			4.5 to 5.5 V		32		
Δt/Δv	Input transition rise or fall rate	Data inputs	1.65 to 1.95 V		20		ns/V
			2.3 to 2.7 V		20		
			3 to 3.6 V		10		
			4.5 to 5.5 V		5		
T _A	Operating free-air temperature				-55	125	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) All unused control inputs must be held at V_{CCA} or GND to ensure proper device operation and minimize power consumption.

(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.

(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

7.4 Thermal Information PW, DW and RHL

THERMAL METRIC ⁽¹⁾	SN74LVC8T245-EP			UNIT
	PW	DW	RHL	
	24 PINS	24 PINS	24 PINS	
R _{θJA} Junction-to-ambient thermal resistance	90.6	68.1	36.2	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	27.6	35.6	27.9	°C/W
R _{θJB} Junction-to-board thermal resistance	45.3	37.8	13.5	°C/W
ψ _{JT} Junction-to-top characterization parameter	1.3	13	0.5	°C/W
ψ _{JB} Junction-to-board characterization parameter	44.8	37.5	13.4	°C/W
R _{θJC(bot)} Junction-to-case (bottom) thermal resistance	N/A	N/A	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			T _A = -55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -100 μA, V _I = V _{IH}	1.65 V to 4.5 V	1.65 V to 4.5 V				V _{CCO} - 0.1		V
	I _{OH} = -4 mA, V _I = V _{IH}	1.65 V	1.65 V				1.2		
	I _{OH} = -8 mA, V _I = V _{IH}	2.3 V	2.3 V				1.9		
	I _{OH} = -24 mA, V _I = V _{IH}	3 V	3 V				2.4		
	I _{OH} = -32 mA, V _I = V _{IH}	4.5 V	4.5 V				3.8		
V _{OL}	I _{OL} = 100 μA, V _I = V _{IL}	1.65 V to 4.5 V	1.65 V to 4.5 V				0.1		V
	I _{OL} = 4 mA, V _I = V _{IL}	1.65 V	1.65 V				0.45		
	I _{OL} = 8 mA, V _I = V _{IL}	2.3 V	2.3 V				0.3		
	I _{OL} = 24 mA, V _I = V _{IL}	3 V	3 V				0.55		
	I _{OL} = 32 mA, V _I = V _{IL}	4.5 V	4.5 V				0.55		
I _I DIR	V _I = V _{CCA} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V	-1	1		-2	2	μA
I _{off} A or B port	V _I or V _O = 0 to 5.5 V	0 V	0 V to 5.5 V	-1	1		-11	11	μA
		0 V to 5.5 V	0 V	-1	1		-11	11	
I _{OZ} A or B port	V _O = V _{CCO} or GND, OE = V _{IH}	1.65 V to 5.5 V	1.65 V to 5.5 V	-1	1		-6	6	μA
I _{CCA}	V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				20		μA
		5 V	0 V				20		
		0 V	5 V				-10		
I _{CCB}	V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				20		μA
		5 V	0 V				-10		
		0 V	5 V				20		
I _{CCA} + I _{CCB}	V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				40		μA
ΔI _{CCA}	A port	One A port at V _{CCA} - 0.6 V, DIR at V _{CCA} , B port = open					50		μA
	DIR	DIR at V _{CCA} - 0.6 V, B port = open, A port at V _{CCA} or GND	3 V to 5.5 V	3 V to 5.5 V			50		
ΔI _{CCB}	B port	One B port at V _{CCB} - 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V			50		μA
C _i Control inputs	V _I = V _{CCA} or GND	3.3 V	3.3 V		4		5		pF
C _{io} A or B port	V _O = V _{CCA/B} or GND	3.3 V	3.3 V		8.5		10		pF

(1) V_{CCO} is the V_{CC} associated with the output port.

(2) V_{CCI} is the V_{CC} associated with the input port.

7.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.7	25.9	1.3	13.2	1	11.4	0.8	11.1	ns
t_{PHL}											
t_{PLH}	B	A	0.9	28.8	0.8	27.6	0.7	27.4	0.7	27.4	ns
t_{PHL}											
t_{PHZ}	\overline{OE}	A	1.5	33.6	1.5	33.4	1.5	33.3	1.4	33.2	ns
t_{PLZ}											
t_{PHZ}	\overline{OE}	B	2.4	36.2	1.9	17.1	1.7	16	1.3	14.3	ns
t_{PLZ}											
t_{PZH}	\overline{OE}	A	0.4	28	0.4	27.8	0.4	27.7	0.4	27.7	ns
t_{PZL}											
t_{PZH}	\overline{OE}	B	1.8	40	1.5	20	1.2	16.6	0.9	14.8	ns
t_{PZL}											

7.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	25.4	1.2	13	0.8	10.2	0.6	8.8	ns
t_{PHL}											
t_{PLH}	B	A	1.2	13.3	1	13.1	1	12.9	0.9	12.8	ns
t_{PHL}											
t_{PHZ}	\overline{OE}	A	1.4	13	1.4	13	1.4	13	1.4	13	ns
t_{PLZ}											
t_{PHZ}	\overline{OE}	B	2.3	33.6	1.8	15	1.7	14.3	0.9	10.9	ns
t_{PLZ}											
t_{PZH}	\overline{OE}	A	1	17.2	1	17.3	1	17.2	1	17.3	ns
t_{PZL}											
t_{PZH}	\overline{OE}	B	1.7	32.2	1.5	18.1	1.2	14.1	1	11.2	ns
t_{PZL}											

7.8 Switching Characteristics

 over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	25.2	1.1	12.8	0.8	10.3	0.5	10.4	ns
t_{PHL}											
t_{PLH}	B	A	0.8	11.2	0.8	10.2	0.7	10.1	0.6	10	ns
t_{PHL}											
t_{PHZ}	\overline{OE}	A	1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	ns
t_{PLZ}											
t_{PHZ}	\overline{OE}	B	2.1	33	1.7	14.3	1.5	12.6	0.8	10.3	ns
t_{PLZ}											
t_{PZH}	\overline{OE}	A	0.8	14.1	0.8	13.6	0.8	13.2	0.8	13.6	ns
t_{PZL}											
t_{PZH}	\overline{OE}	B	1.8	31.7	1.4	18.4	1.1	12.9	0.9	10.9	ns
t_{PZL}											

7.9 Switching Characteristics

 over recommended operating free-air temperature range, $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	25.4	1	12.8	0.7	10	0.4	8.2	ns
t_{PHL}											
t_{PLH}	B	A	0.7	11	0.4	8.8	0.3	8.5	0.3	8.3	ns
t_{PHL}											
t_{PHZ}	\overline{OE}	A	0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	ns
t_{PLZ}											
t_{PHZ}	\overline{OE}	B	2	32.7	1.6	13.7	1.4	12	0.7	9.7	ns
t_{PLZ}											
t_{PZH}	\overline{OE}	A	0.7	10.9	0.7	10.9	0.7	10.9	0.7	10.9	ns
t_{PZL}											
t_{PZH}	\overline{OE}	B	1.5	31.6	1.3	18.4	1	13.7	0.9	10.7	ns
t_{PZL}											

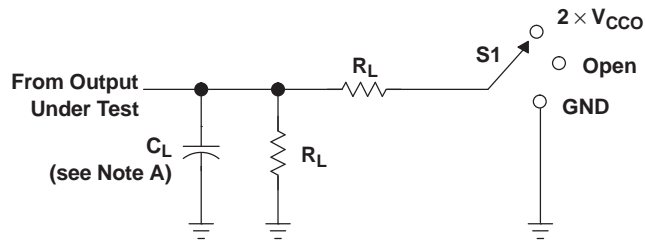
7.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.8 \text{ V}$	$V_{CCA} = V_{CCB} = 2.5 \text{ V}$	$V_{CCA} = V_{CCB} = 3.3 \text{ V}$	$V_{CCA} = V_{CCB} = 5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	2	2	2	3	pF
	B-port input, A-port output	12	13	13	16	
C_{pdB} (1)	A-port input, B-port output	13	13	14	16	pF
	B-port input, A-port output	2	2	2	3	

(1) Power dissipation capacitance per transceiver

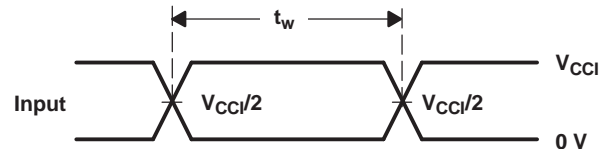
8 Parameter Measurement Information



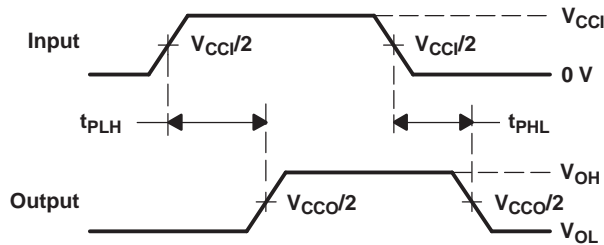
LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V

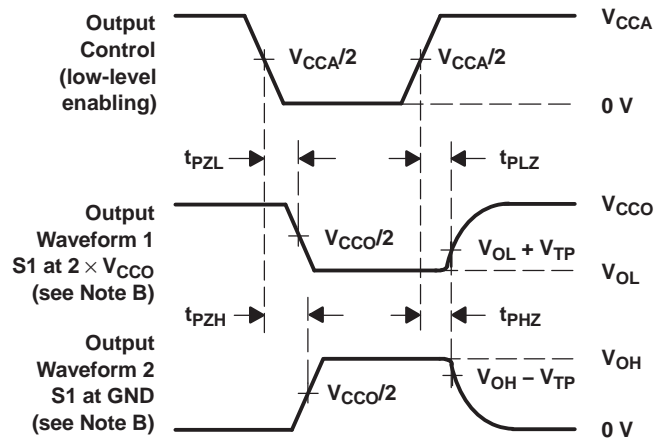
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. V_{CCI} is the V_{CC} associated with the input port.
 - I. V_{CCO} is the V_{CC} associated with the output port.
 - J. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVC8T245-EP device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum output current can be up to 32 mA when device is powered by 5 V.

10.2 Typical Application

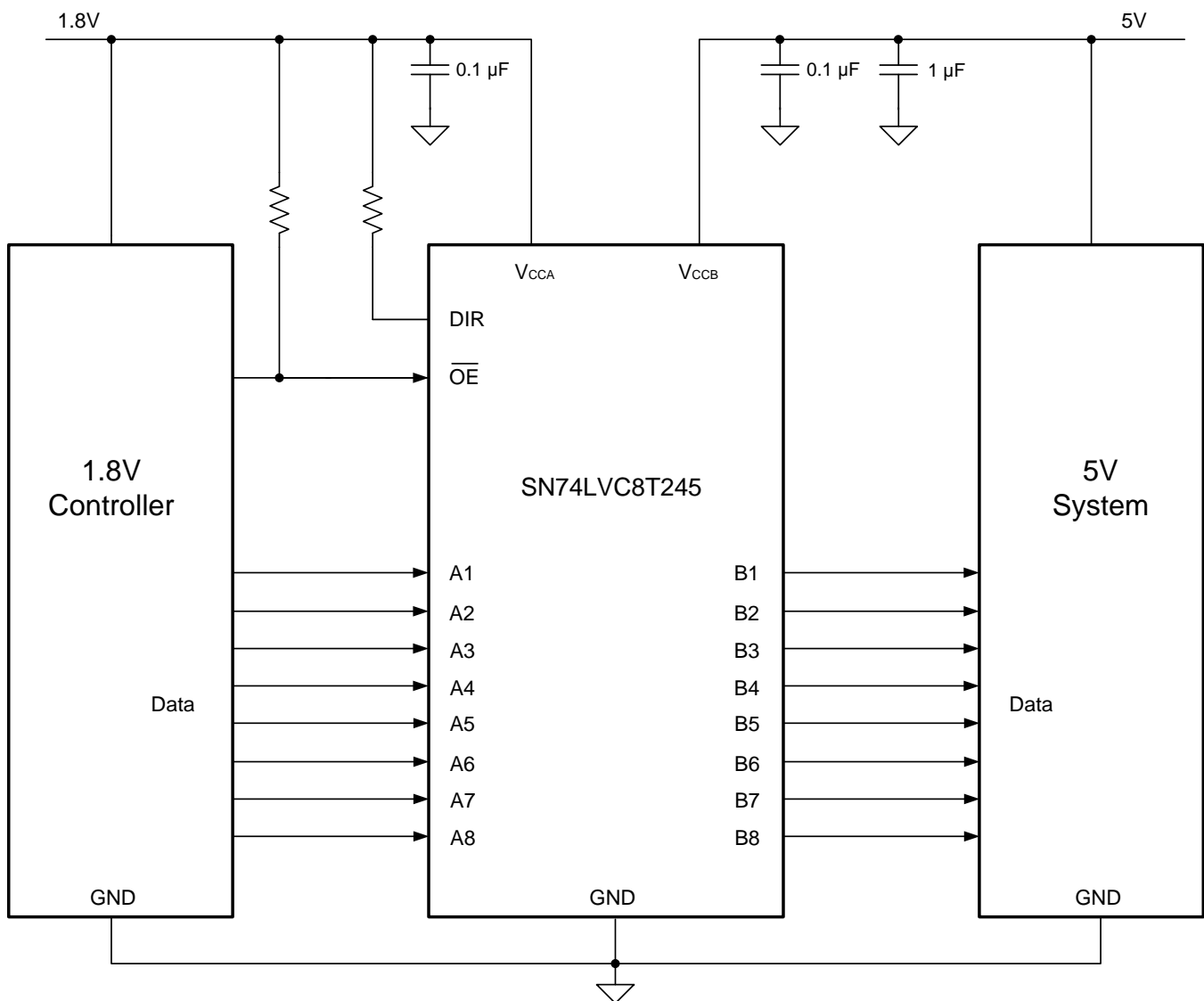


Figure 3. Typical Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#).

Table 2. Design Parameters

PARAMETERS	VALUES
Input voltage range	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the SN74LVC8T245-EP device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74LVC8T245-EP device is driving to determine the output voltage range.

10.2.3 Application Curve

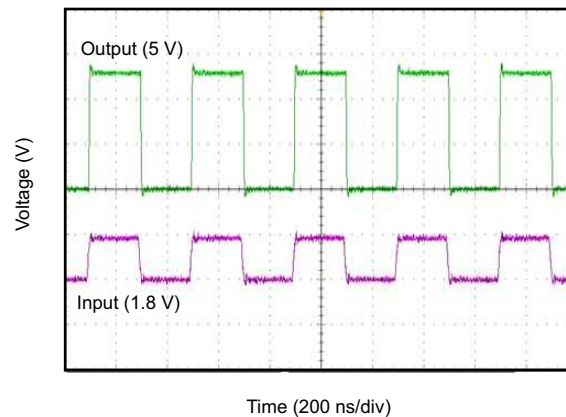


Figure 4. Translation Up (1.8 V to 5 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74LVC8T245-EP device uses two separate configurable power-supply rails, VCCA and VCCB. VCCA accepts any supply voltage from 1.65 V to 5.5 V and VCCB accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track VCCA and VCCB respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5 -V, 3.3-V and 5-V voltage nodes.

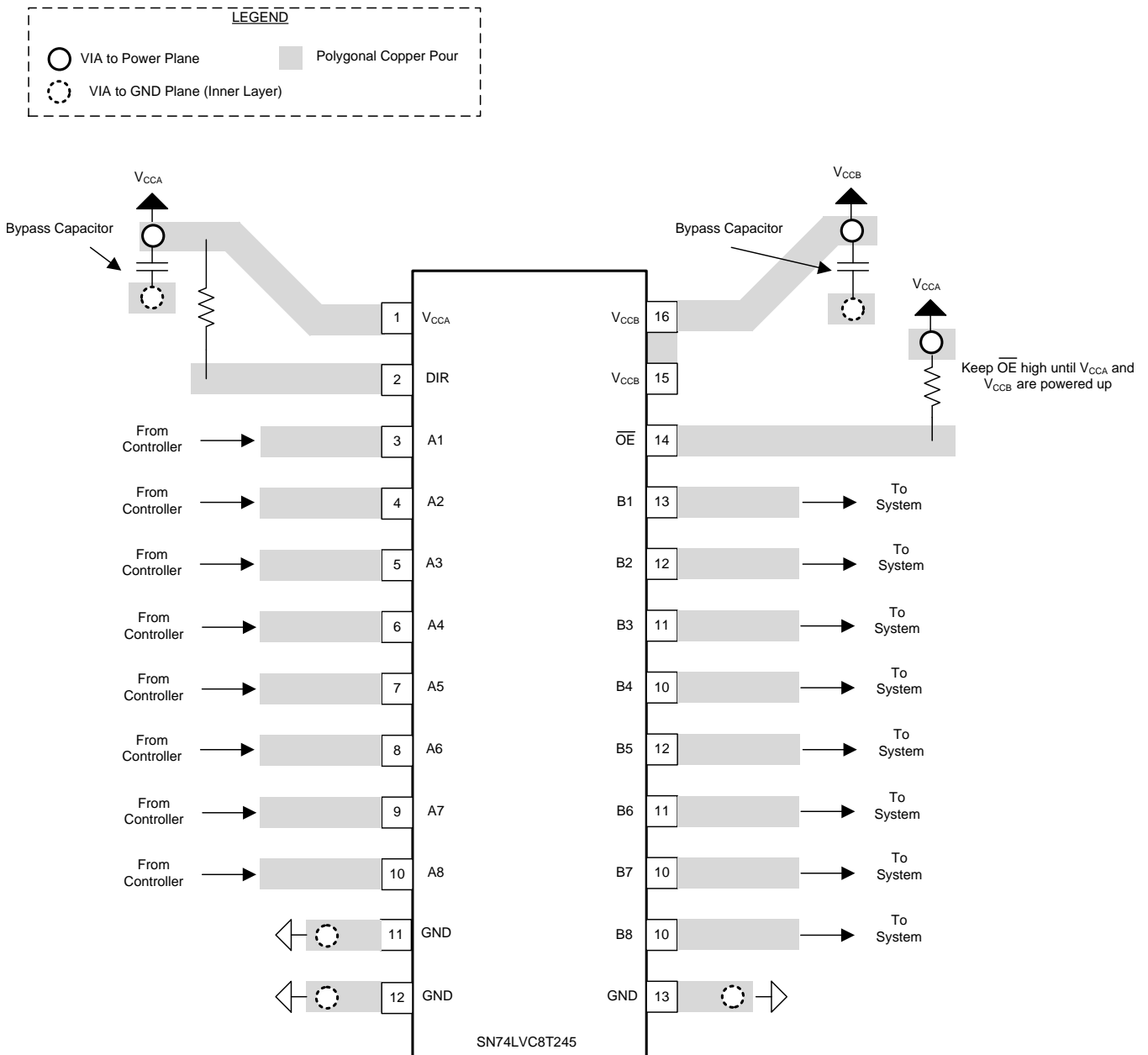
12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

12.2 Layout Example



13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC8T245MRHLTEP	ACTIVE	VQFN	RHL	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	P8T245M	Samples
SN74LVC8T245MDWREP	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	LVC8T245M	Samples
SN74LVC8T245MPWREP	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	NH245MEP	Samples
V62/09615-01XE	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	NH245MEP	Samples
V62/09615-01YE	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	LVC8T245M	Samples
V62/09615-01ZE	ACTIVE	VQFN	RHL	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	P8T245M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC8T245-EP :

- Catalog: [SN74LVC8T245](#)
- Automotive: [SN74LVC8T245-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC8T245MRHLTEP	VQFN	RHL	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74LVC8T245MDWREP	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC8T245MRHLTEP	VQFN	RHL	24	250	210.0	185.0	35.0
SN74LVC8T245MDWREP	SOIC	DW	24	2000	367.0	367.0	45.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

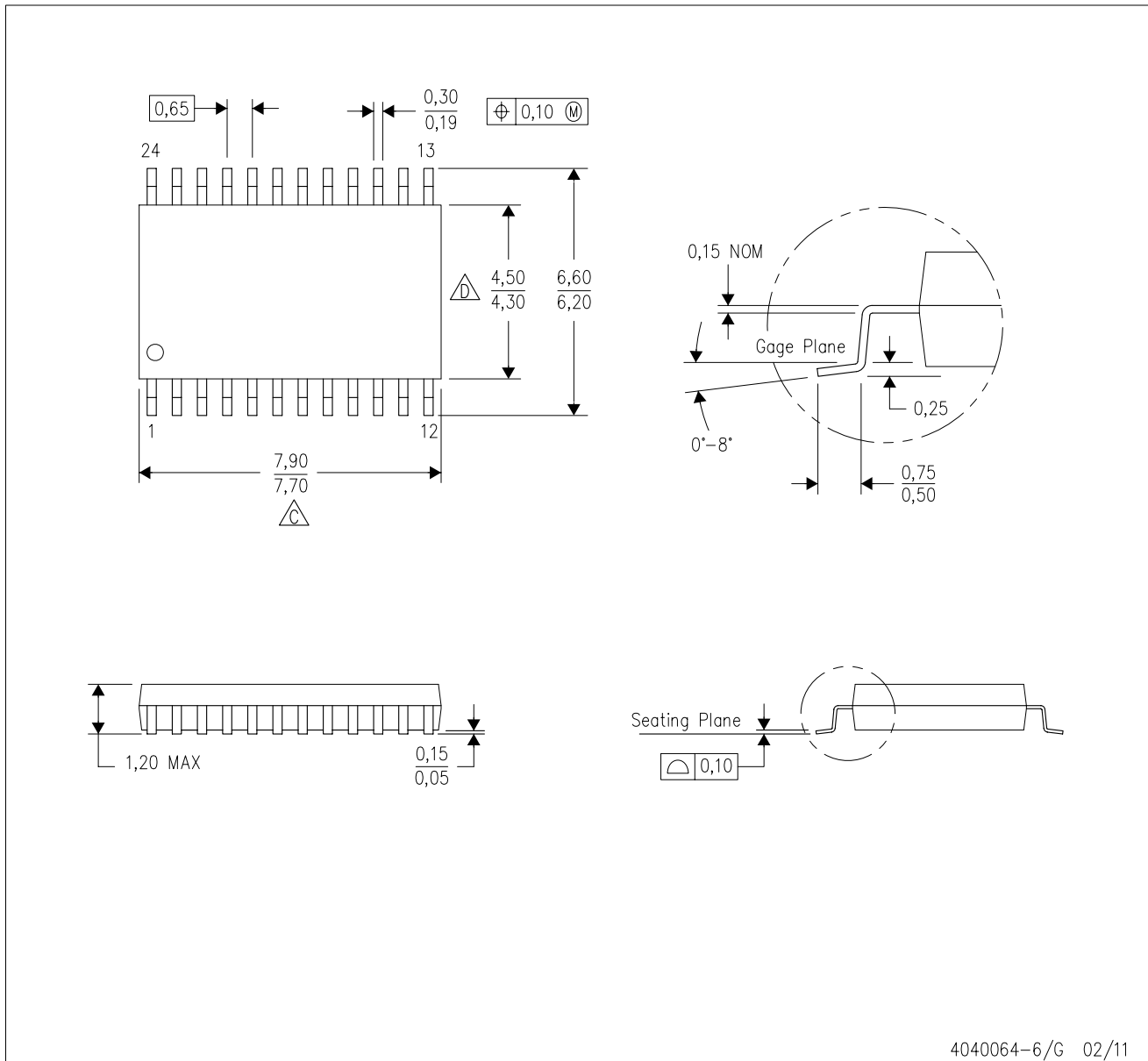




- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

MECHANICAL DATA

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



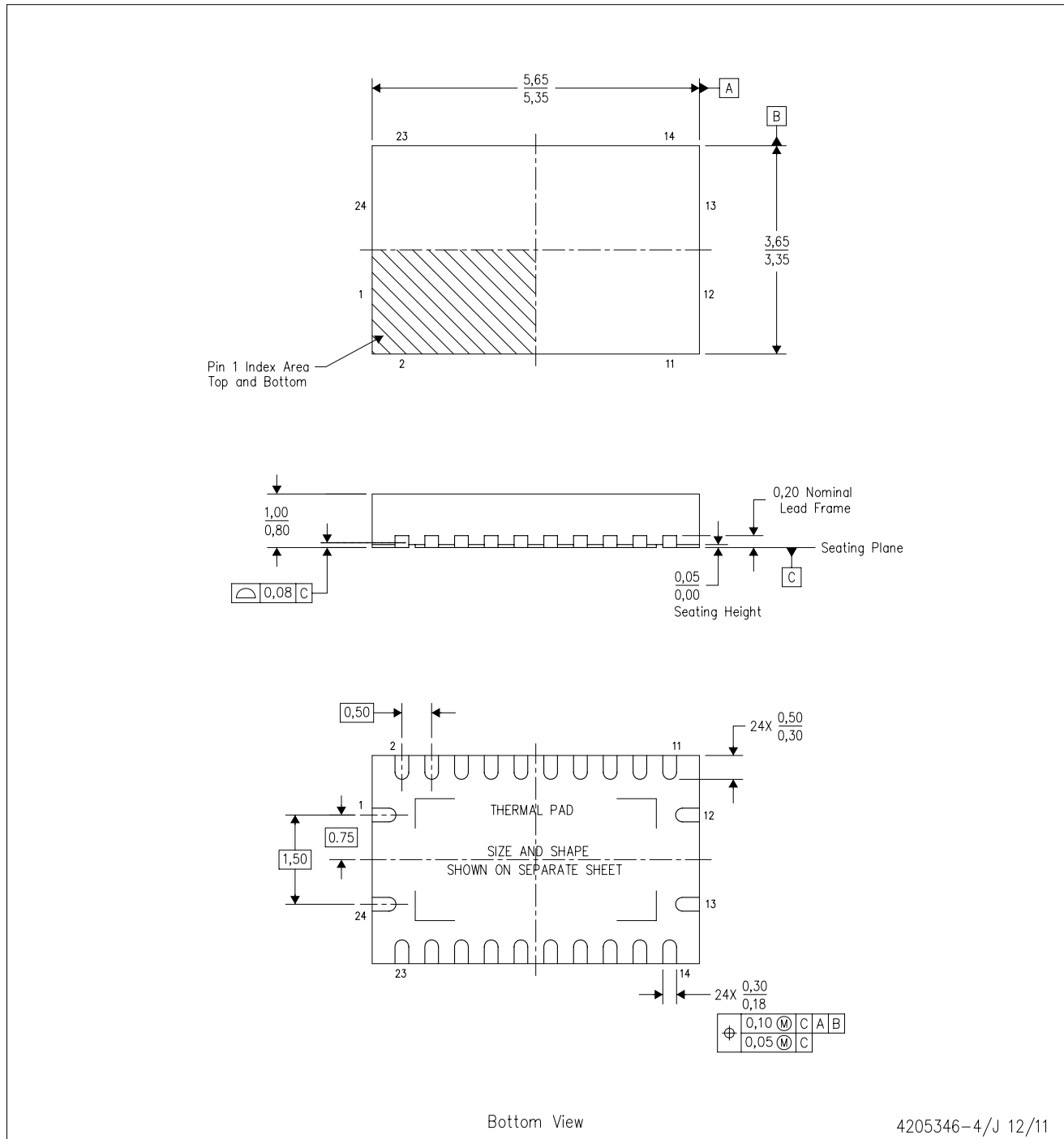
4211284-4/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

RHL (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - JEDEC MO-241 package registration pending.

THERMAL PAD MECHANICAL DATA

RHL (S-PVQFN-N24)

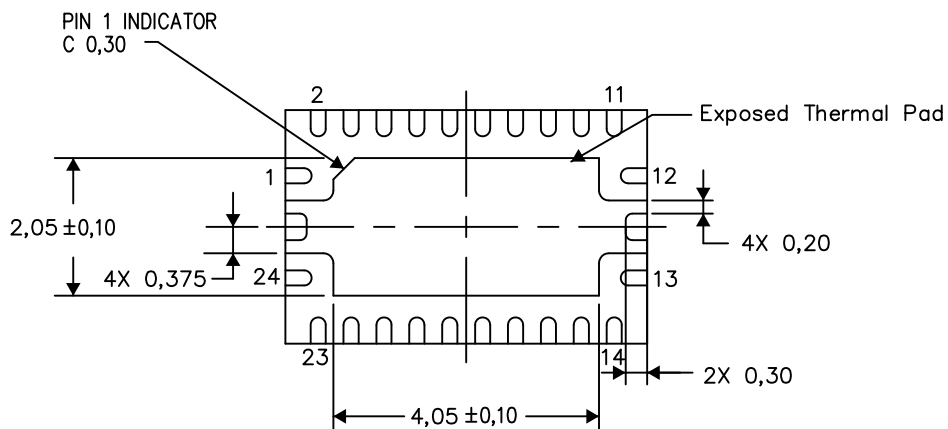
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

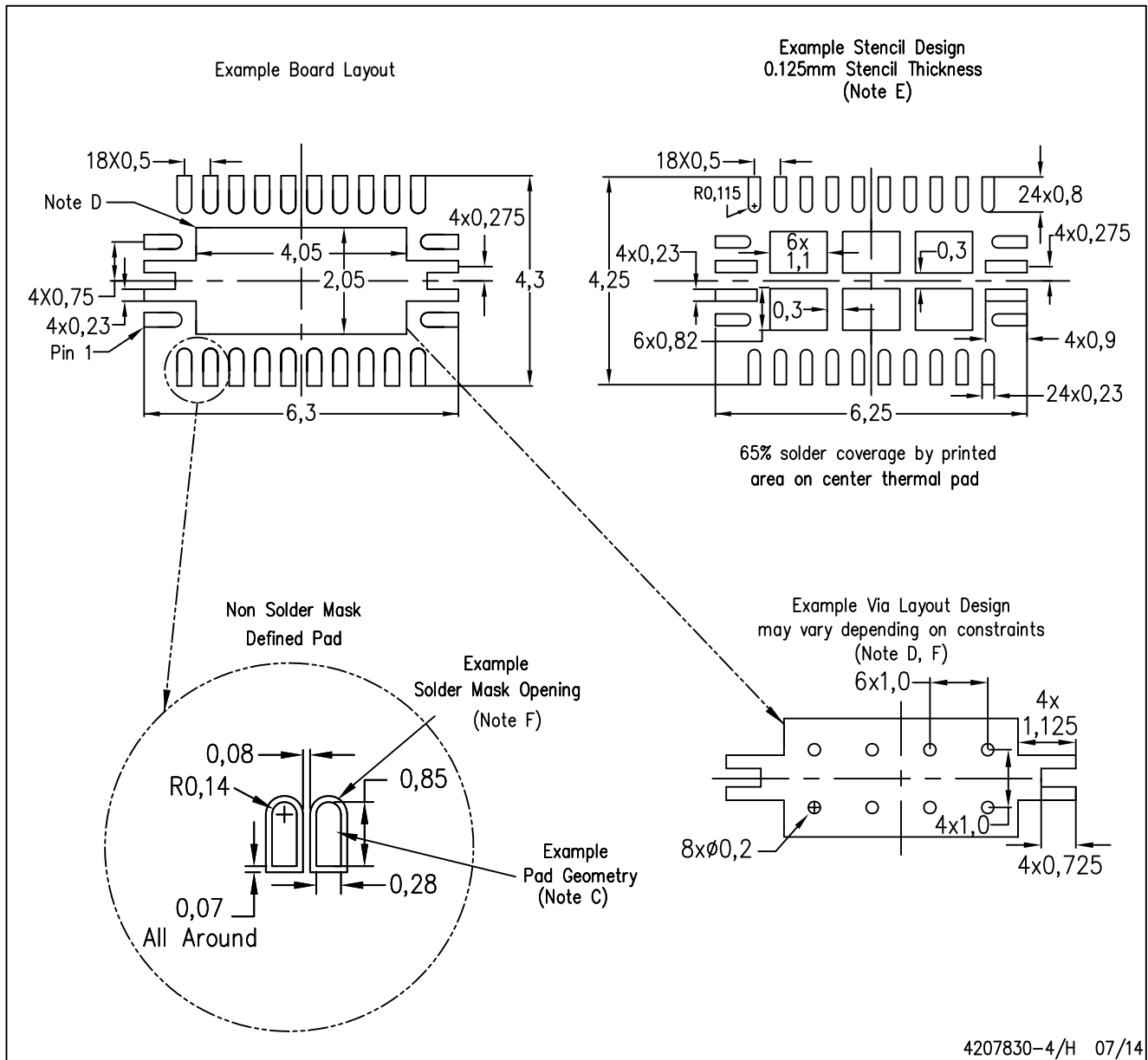
Exposed Thermal Pad Dimensions

4206363-4/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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