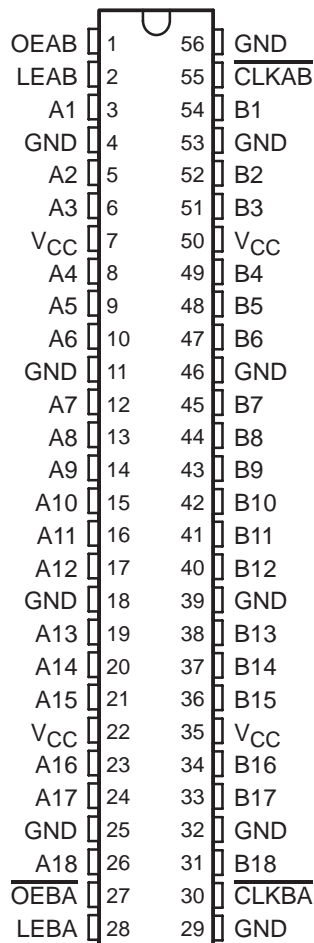


SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments Widebus™ Family
- UBT™ Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVTH16500 . . . WD PACKAGE
SN74LVTH16500 . . . DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVTH16500DL	LVTH16500
		Tape and reel	SN74LVTH16500DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH16500DGGR	LVTH16500
	VFBGA – GQL	Tape and reel	SN74LVTH16500GQLR	LL500
VFBGA – ZQL (Pb-free)	SN74LVTH16500ZQLR			
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16500WD	SNJ54LVTH16500WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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SN54LVTH16500, SN74LVTH16500

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description/ordering information (continued)

Data flow in each direction is controlled by output-enable (\overline{OEBA} and \overline{OEAB}), latch-enable (LEAB and LEBA), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

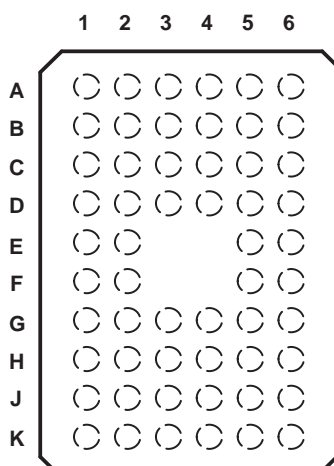
Data flow for B to A is similar to that of A to B, but uses $\overline{OEB\bar{A}}$, LEBA, and \overline{CLKBA} . The output enables are complementary (OEAB is active high and $\overline{OEB\bar{A}}$ is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	A1	LEAB	OEAB	GND	\overline{CLKAB}	B1
B	A3	A2	GND	GND	B2	B3
C	A5	A4	V_{CC}	V_{CC}	B4	B5
D	A7	A6	GND	GND	B6	B7
E	A9	A8			B8	B9
F	A10	A11			B11	B10
G	A12	A13	GND	GND	B13	B12
H	A14	A15	V_{CC}	V_{CC}	B15	B14
J	A16	A17	GND	GND	B17	B16
K	A18	$\overline{OEB\bar{A}}$	LEBA	GND	\overline{CLKBA}	B18

SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE†

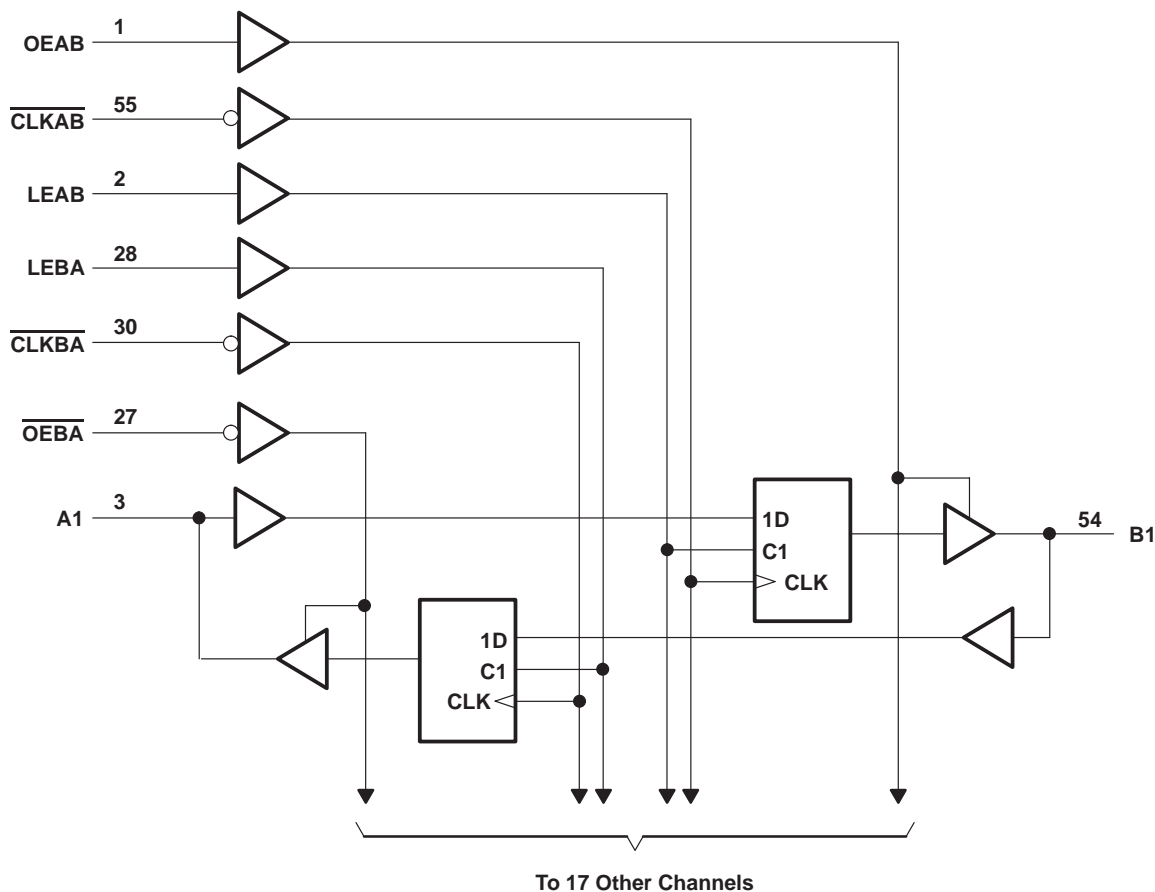
INPUTS				OUTPUT B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ ‡
H	L	L	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

SN54LVTH16500, SN74LVTH16500

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16500	96 mA
SN74LVTH16500	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16500	48 mA
SN74LVTH16500	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DL package	56°C/W
GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

	SN54LVTH16500		SN74LVTH16500		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		-24		-32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200		200		μ s/V
T_A Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH16500		SN74LVTH16500		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			V
V_{OH}		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$		$V_{CC}-0.2$		V	
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4		2.4			
		$V_{CC} = 3\text{ V}$	2		2			
V_{OL}		$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2	0.2	V	
			$I_{OL} = 24\text{ mA}$		0.5	0.5		
		$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4	0.4		
			$I_{OL} = 32\text{ mA}$		0.5	0.5		
			$I_{OL} = 48\text{ mA}$		0.55			
			$I_{OL} = 64\text{ mA}$			0.55		
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1	± 1	μA		
		$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$		10	10			
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		20	20			
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		1	1			
		$V_I = 0$		-5	-5			
I_{off}		$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$			± 100	μA		
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75	75	μA		
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$		-75	-75			
		$V_{CC} = 3.6\text{ V}\S$, $V_I = 0\text{ to }3.6\text{ V}$			± 500			
I_{OZPU}		$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$		$\pm 100^*$	± 100	μA		
I_{OZPD}		$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$		$\pm 100^*$	± 100	μA		
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$		Outputs high		0.19	0.19	mA	
			Outputs low		5	5		
			Outputs disabled		0.19	0.19		
$\Delta I_{CC}\P$		$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2	0.2	mA		
C_i		$V_I = 3\text{ V or }0$		4	4	pF		
C_{iO}		$V_O = 3\text{ V or }0$		10	10	pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}\text{ or GND}$.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVTH16500, SN74LVTH16500

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH16500				SN74LVTH16500				UNIT	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency	150		150		150		150		MHz	
t_w	Pulse duration	LE high		3.3		3.3		3.3		ns	
		$\overline{\text{CLK}}$ high or low		3.3		3.3		3.3			
t_{su}	Setup time	A before $\overline{\text{CLKAB}}\downarrow$		3.1		3.1		2.9		ns	
		B before $\overline{\text{CLKBA}}\downarrow$		3.1		3.1		2.9			
		A or B before LE \downarrow	$\overline{\text{CLK}}$ high		1.5		0.6		1.4		
			$\overline{\text{CLK}}$ low		3.1		2.5		2.9		
t_h	Hold time	A or B after $\overline{\text{CLK}}\downarrow$		0.4		0.4		0.4		ns	
		A or B after LE \downarrow		1.7		1.7		1.6			

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16500				SN74LVTH16500				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f_{max}			150		150		150		150		MHz
t_{PLH}	B or A	A or B	1.2 3.9		4.1		1.3 2.8 3.7		4		ns
t_{PHL}			1.2 3.9		4.1		1.3 2.6 3.7		4		
t_{PLH}	LEBA or LEAB	A or B	1.4 5.5		5.9		1.5 3.8 5.1		5.7		ns
t_{PHL}			1.4 5.5		5.9		1.5 3.8 5.1		5.7		
t_{PLH}	$\overline{\text{CLKBA}}$ or $\overline{\text{CLKAB}}$	A or B	1.2 5.3		6.1		1.3 3.6 5		5.9		ns
t_{PHL}			1.2 5.3		6.1		1.3 3.5 5		5.9		
t_{PZH}	$\overline{\text{OEBA}}$ or OEAB	A or B	1.2 5.1		5.8		1.3 3.6 4.8		5.5		ns
t_{PZL}			1.2 5.1		5.8		1.3 3.6 4.8		5.5		
t_{PHZ}	$\overline{\text{OEBA}}$ or OEAB	A or B	1.6 6.1		6.6		1.7 4.5 5.8		6.3		ns
t_{PLZ}			1.6 6.1		6.6		1.7 4.1 5.8		6.3		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

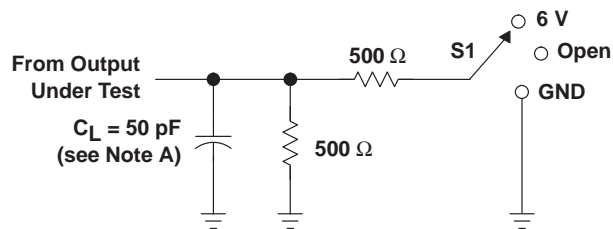
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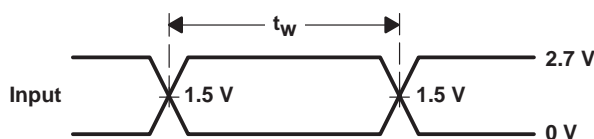
SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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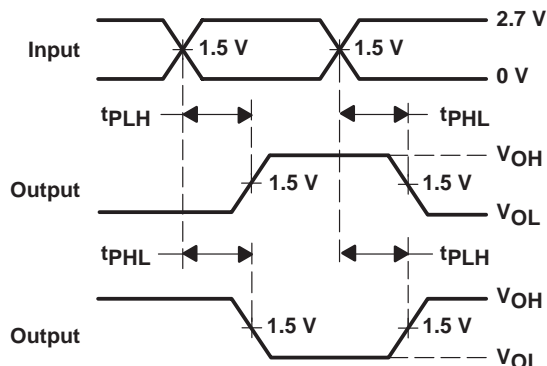
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

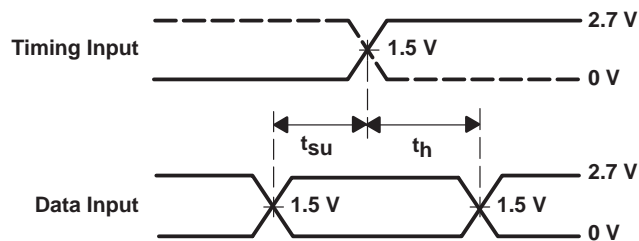


VOLTAGE WAVEFORMS
PULSE DURATION

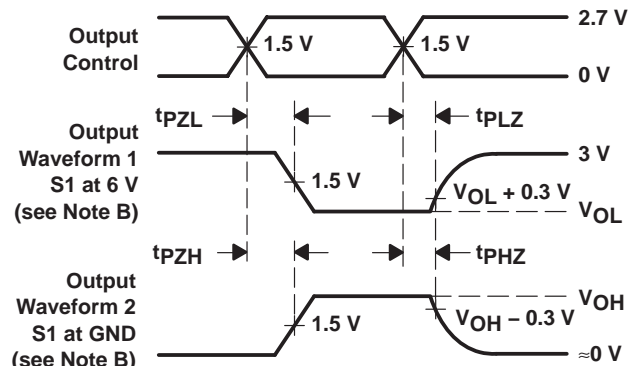


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PHL}/t_{PLH}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVTH16500DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500	Samples
SN74LVTH16500DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16500	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16500DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

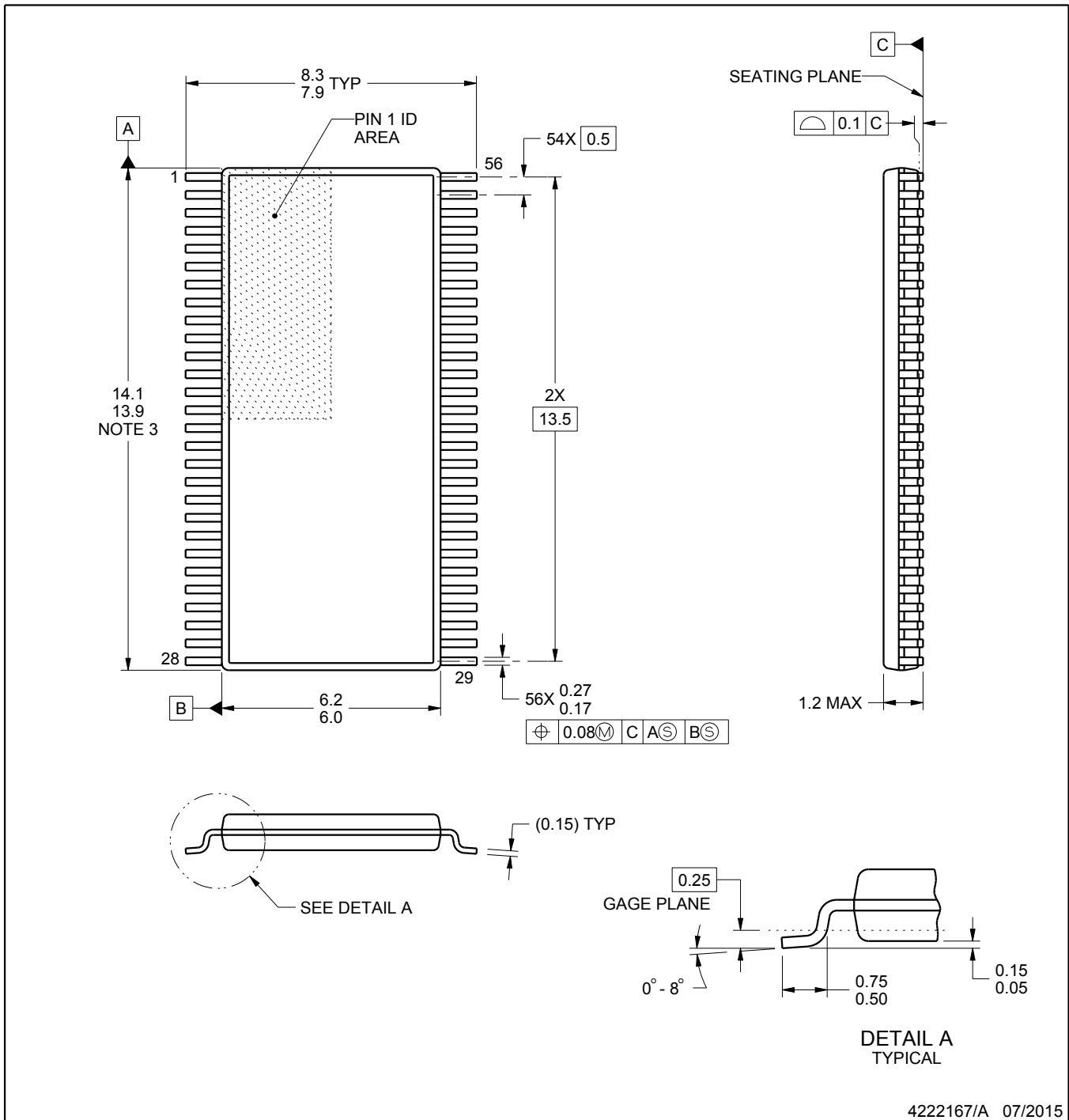
DGG0056A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.