TLV743P 300-mA, Low-Dropout Regulator

1 Features

- Input Voltage Range: 1.4 V to 5.5 V
- Stable Operation With 1-µF Ceramic Output Capacitor
- Foldback Overcurrent Protection
- Packages:
  - SOT-23 (5)
- Very Low Dropout: 125 mV at 300 mA (3.3 V_{OUT})
- Accuracy: 1% (Typical), 1.4% (Maximum)
- Low I_Q: 34 µA
- Available in Fixed-Output Voltages: 1 V to 3.3 V
- High PSRR: 50 dB at 1 kHz
- Active Output Discharge

2 Applications

- Tablets
- Smartphones
- Notebook and Desktop Computers
- Portable Industrial and Consumer Products
- WLAN and Other PC Add-On Cards
- Camera Modules

3 Description

The TLV743P low-dropout linear regulator (LDO) is an ultra-small, low quiescent current LDO that sources 300 mA with good line and load transient performance. The device provides a typical accuracy of 1%.

The TLV743P is designed to be stable with a small output capacitor with a value of 1 µF. The TLV743P device provides foldback current control during device power up and enabling. This functionality is especially important in battery-operated devices.

The TLV743P provides an active pulldown circuit to quickly discharge output loads when the device is disabled.

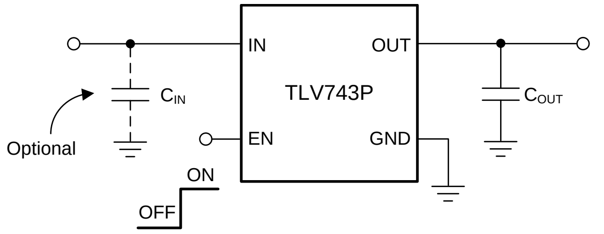
The TLV743P is available in a standard DBV (SOT-23) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV743P	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application Circuit



Dropout Voltage vs Output Current

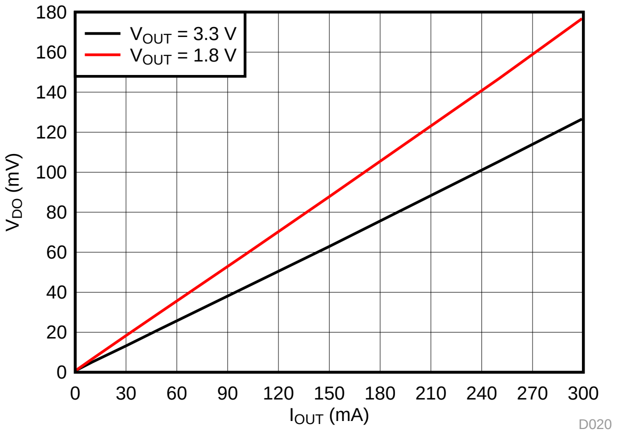


Table of Contents

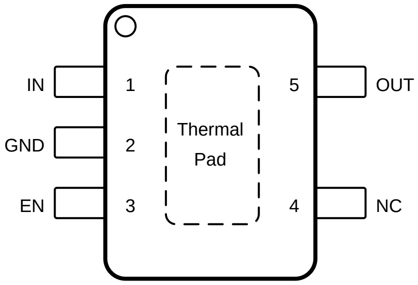
1 **Features** 1
2 **Applications** 1
3 **Description** 1
4 **Revision History** 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 4
6.5 Electrical Characteristics 5
7 **Typical Characteristics** 7
8 **Detailed Description** 12
8.1 Overview 12
8.2 Functional Block Diagram 12
8.3 Feature Description 13
8.4 Device Functional Modes 14
9 **Application and Implementation** 15
9.1 Application Information 15
9.2 Typical Applications 17
10 **Power-Supply Recommendations** 18
11 **Layout** 18
11.1 Layout Guidelines 18
11.2 Layout Examples 18
12 **Device and Documentation Support** 19
12.1 Device Support 19
12.2 Documentation Support 19
12.3 Trademarks 19
12.4 Electrostatic Discharge Caution 19
12.5 Glossary 19
13 **Mechanical, Packaging, and Orderable Information** 20

4 Revision History

DATE	REVISION	NOTES
July 2017	*	Initial release.

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

NC- no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Drive EN greater than 0.9 V to turn on the regulator. Drive EN less than 0.35 V to put the LDO into shutdown mode.
GND	2	—	Ground pin
IN	1	I	Input pin. A small capacitor is recommended from this pin to ground. See *Input and Output Capacitor Selection* for more details.
NC	4	—	No internal connection
OUT	5	O	Regulated output voltage pin. For best transient response, use a small 1-µF ceramic capacitor from this pin to ground. See *Input and Output Capacitor Selection* for more details.
Thermal pad	—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	V_{IN} + 0.3	
	V_{OUT}	–0.3	3.6	
Current	I_{OUT}	Internally limited		A
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	160	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input range	1.4		5.5	V
V_{OUT}	Output range	1		3.3	V
I_{OUT}	Output current	0		300	mA
V_{EN}	Enable range	0		V_{IN}	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV743P	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT}$(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT}$ = 1 µF (unless otherwise noted). All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.4		5.5	V
	DC output accuracy	T_J = 25°C		–1%		1%	
		–40°C ≤ T_J ≤ 125°C		–1.4%		1.4%	
UVLO	Undervoltage lockout	V_{IN} rising			1.3	1.4	V
		V_{IN} falling			1.25		
$\Delta V_{O(\Delta VI)}$	Line regulation	$\Delta VI = V_{IN(nom)}$ to $V_{IN(nom)}$ + 1			1		mV
$\Delta V_{O(\Delta IO)}$	Load regulation	ΔIO = 1 mA to 300 mA	DBV package		16		mV
					25		
V_{DO}	Dropout voltage(1)	$V_{OUT} = 0.98 \times V_{OUT(nom)}$ I_{OUT} = 300 mA	V_{OUT} = 1.1 V –40°C ≤ T_J ≤ 85°C			480	mV
			1.2 V ≤ V_{OUT} < 1.5 V –40°C ≤ T_J ≤ 85°C			420	
			1.5 V ≤ V_{OUT} < 1.8 V –40°C ≤ T_J ≤ 85°C			370	
			1.8 V ≤ V_{OUT} < 2.5 V –40°C ≤ T_J ≤ 85°C			270	
			2.5 V ≤ V_{OUT} < 3.3 V –40°C ≤ T_J ≤ 85°C			260	
			V_{OUT} = 3.3 V –40°C ≤ T_J ≤ 85°C		125	220	
			1.2 V ≤ V_{OUT} < 1.5 V –40°C ≤ T_J ≤ 125°C			450	
			1.5 V ≤ V_{OUT} < 1.8 V –40°C ≤ T_J ≤ 125°C			400	
			1.8 V ≤ V_{OUT} < 2.5 V –40°C ≤ T_J ≤ 125°C			300	
			2.5 V ≤ V_{OUT} < 3.3 V –40°C ≤ T_J ≤ 125°C			290	
			V_{OUT} = 3.3 V –40°C ≤ T_J ≤ 125°C		125	270	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			34	60	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.35 V 2 V ≤ V_{IN} ≤ 5.5 V T_J = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8 V I_{OUT} = 300 mA	f = 100 Hz		68		dB
			f = 10 kHz		35		
			f = 100 kHz		28		
V_n	Output noise voltage	Bandwidth = 10 Hz to 100 kHz V_{OUT} = 1.8 V I_{OUT} = 10 mA			120		μV_{RMS}
$V_{EN(HI)}$	EN pin high voltage (enabled)			0.9	0.63		V
$V_{EN(LO)}$	EN pin low voltage (disabled)				0.52	0.35	V
I_{EN}	EN pin current	V_{EN} = 5.5 V			0.01		µA

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(1) Dropout voltage for the TLV743P is not valid at room temperature. The device engages undervoltage lockout ($V_{IN} < UVLO_{FALL}$) before the dropout condition is met.

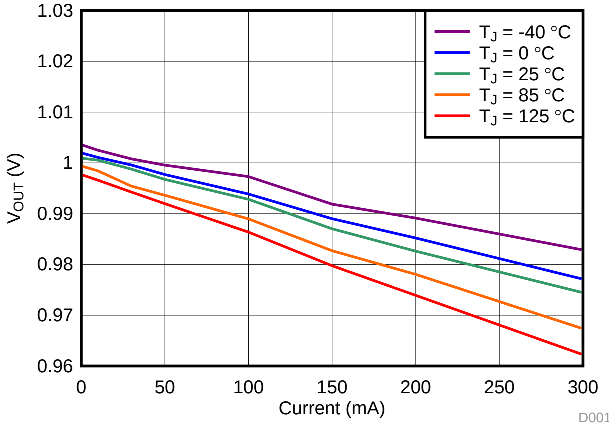
Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted). All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Startup time	Time from EN assertion to 98% × V_{OUT}(nom) V_{OUT} = 1 V I_{OUT} = 0 mA		250		µs
		Time from EN assertion to 98% × V_{OUT}(nom) V_{OUT} = 3.3 V I_{OUT} = 0 mA		800		
	Pulldown resistor	V_{IN} = 2.3 V		120		Ω
I_{LIM}	Output current limit		360			mA
I_{OS}	Short-circuit current limit	V_{OUT} shorted to GND V_{OUT} = 1 V		150		mA
		V_{OUT} shorted to GND V_{OUT} = 3.3 V		170		
T_{sd}	Thermal shutdown	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

7 Typical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



TLV74310PDBV

Figure 1. 1-V Load Regulation vs I_{OUT} and Temperature

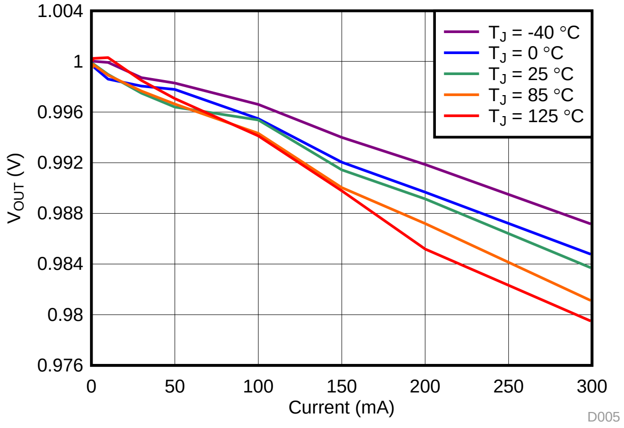
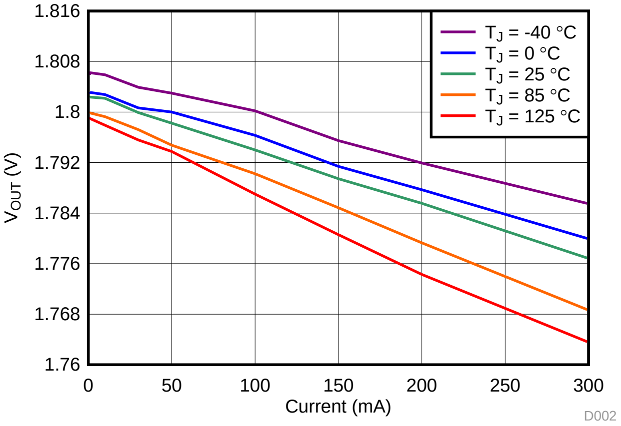


Figure 2. 1-V Load Regulation vs I_{OUT} and Temperature



TLV74318PDBV

Figure 3. 1.8-V Load Regulation vs I_O and Temperature

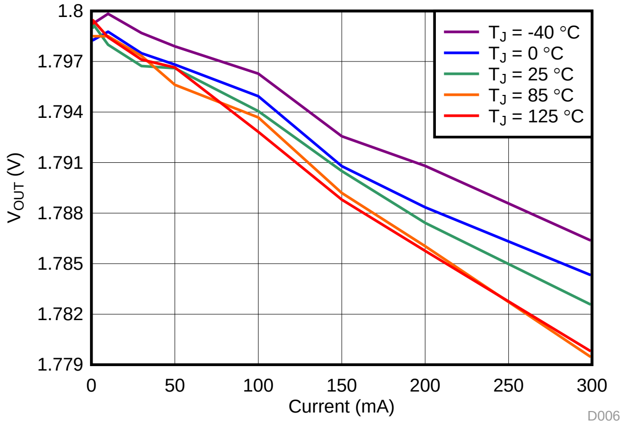
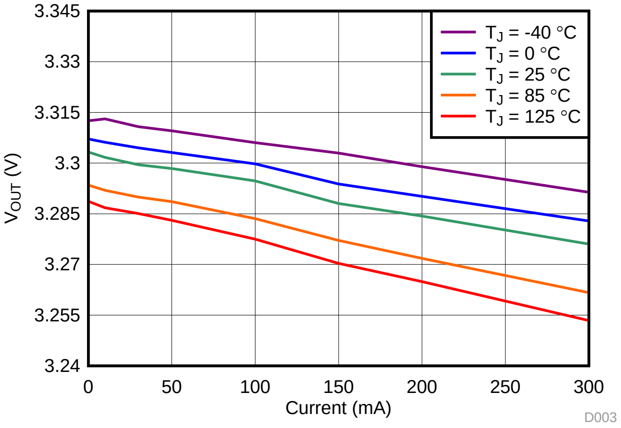


Figure 4. 1.8-V Load Regulation vs I_{OUT} and Temperature



TLV74333PDBV

Figure 5. 3.3-V Load Regulation vs I_{OUT} and Temperature

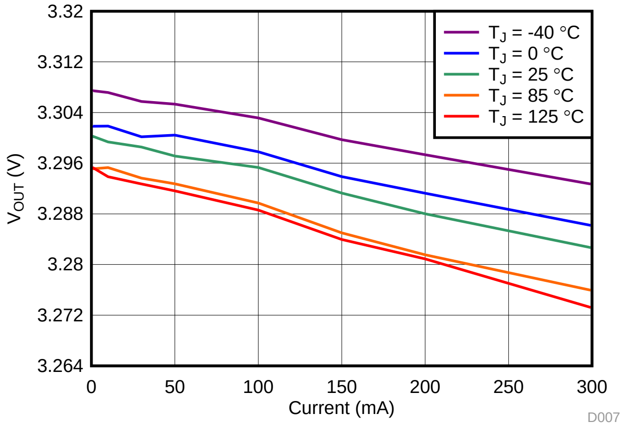
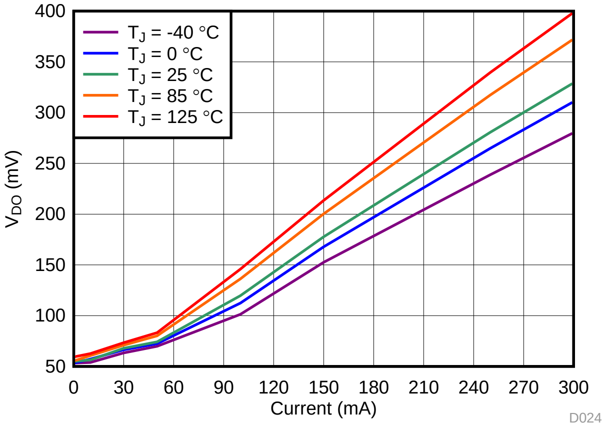


Figure 6. 3.3-V Load Regulation vs I_{OUT} and Temperature

Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



TLV74312PDBV

Figure 7. 1.2-V Dropout Voltage vs I_{OUT} and Temperature

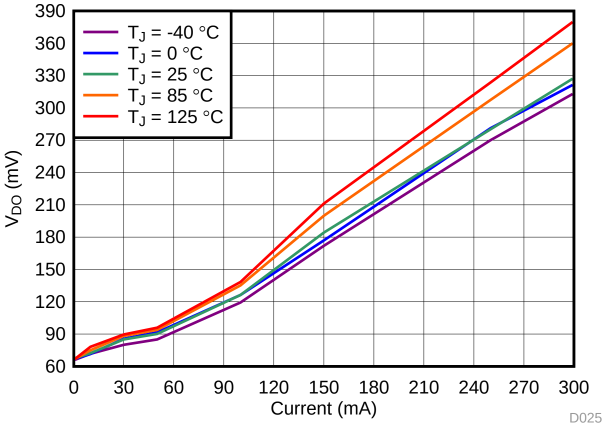
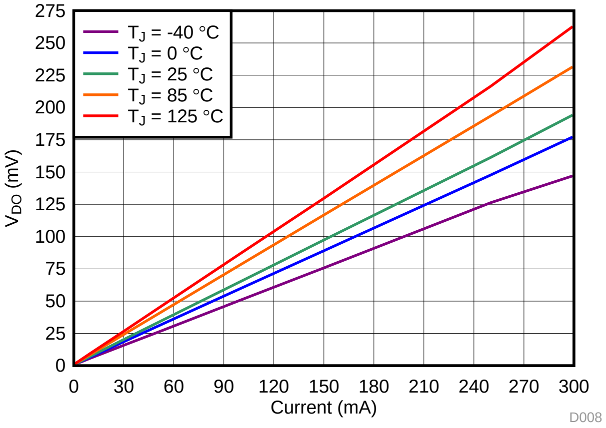


Figure 8. 1.2-V Dropout Voltage vs I_{OUT} and Temperature



TLV74318PDBV

Figure 9. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

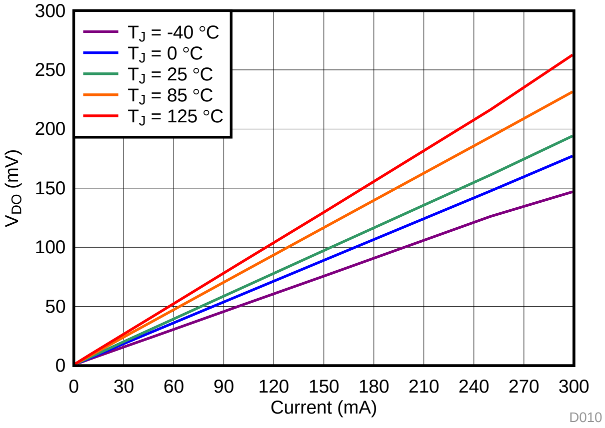
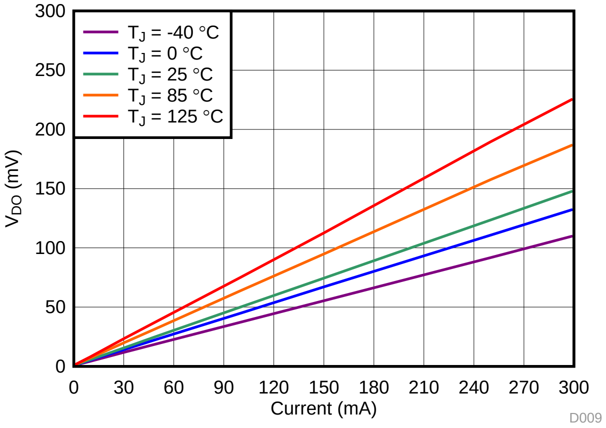


Figure 10. 1.8-V Dropout Voltage vs I_{OUT} and Temperature



TLV74333PDBV

Figure 11. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

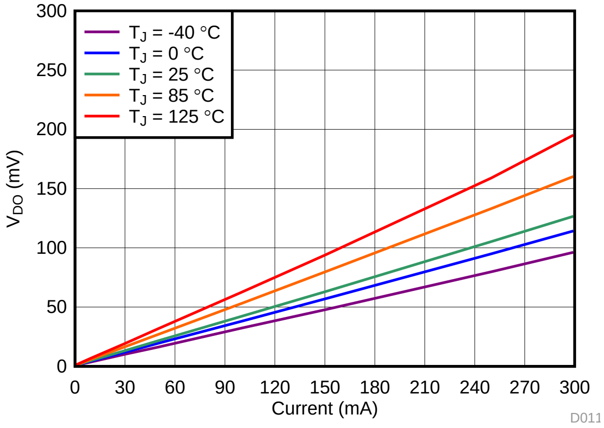


Figure 12. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT}$(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT}$ = 1 µF (unless otherwise noted)

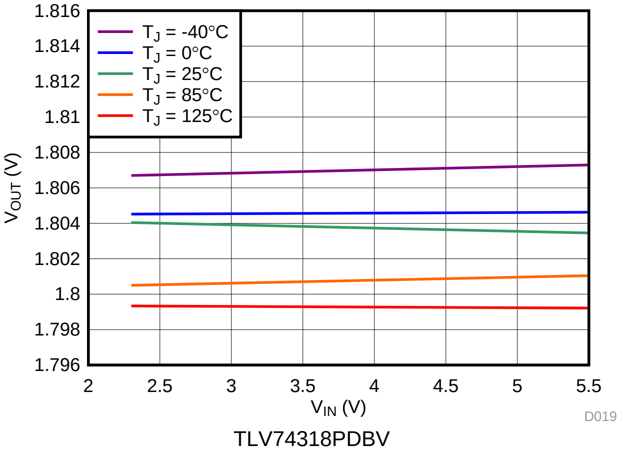


Figure 13. 1.8-V Regulation vs V_{IN} (Line Regulation) and Temperature

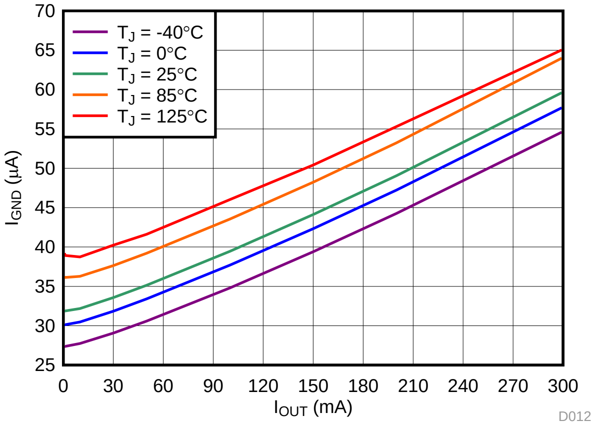


Figure 14. Ground Pin Current vs I_{OUT} and Temperature

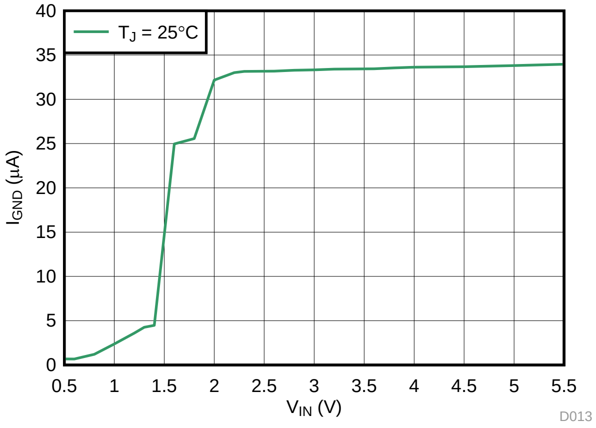


Figure 15. Ground Pin Current vs V_{IN}

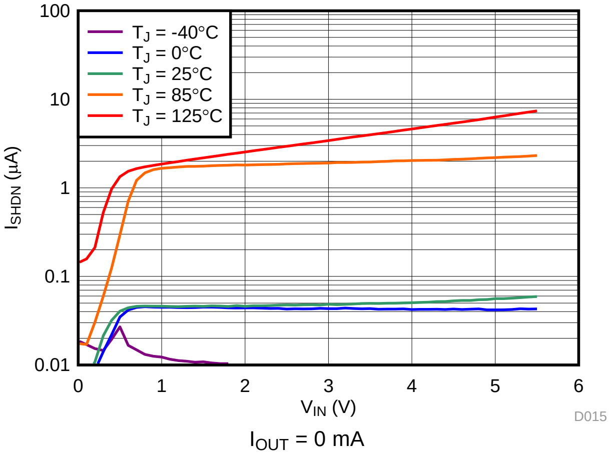


Figure 16. Shutdown Current vs V_{IN} and Temperature

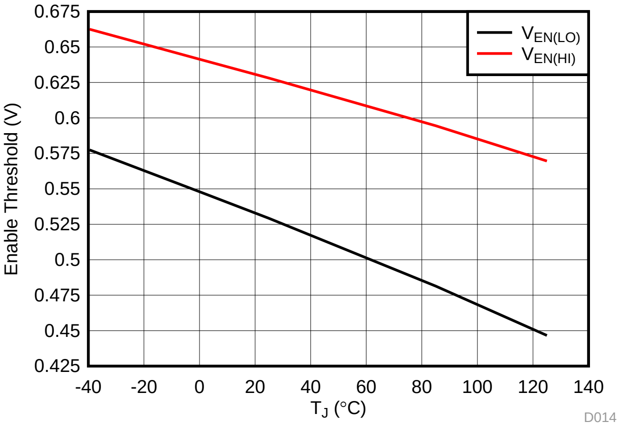


Figure 17. Enable Threshold vs Temperature

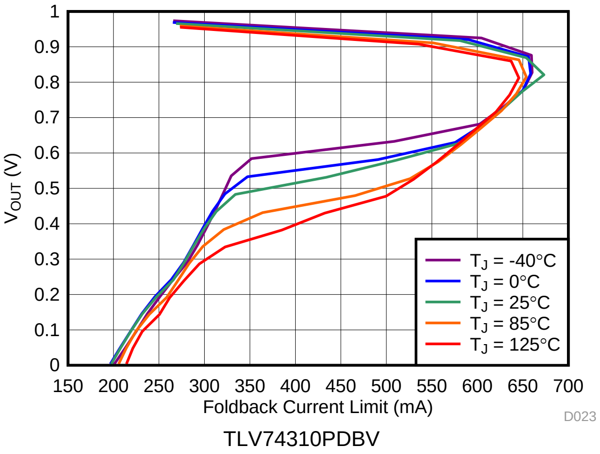
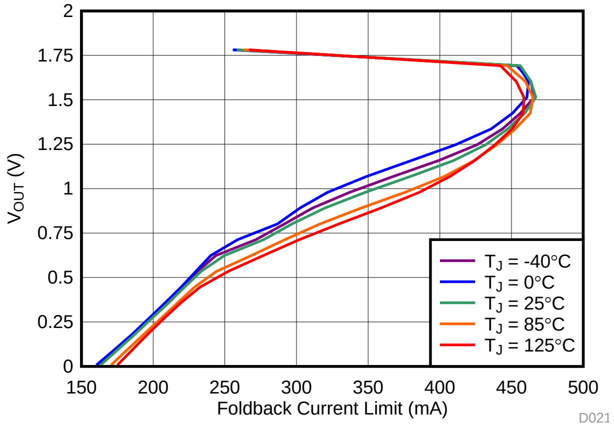


Figure 18. 1-V Foldback Current Limit vs I_{OUT} and Temperature

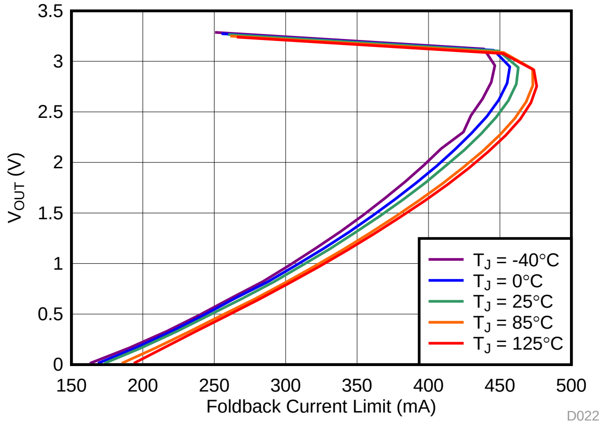
Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



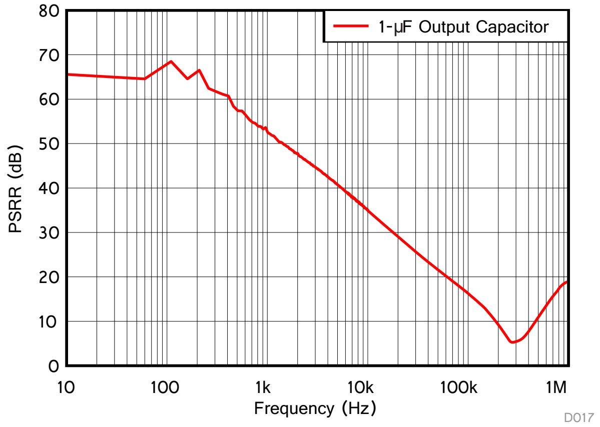
TLV74318PDBV

Figure 19. 1.8-V Foldback Current Limit vs I_{OUT} and Temperature



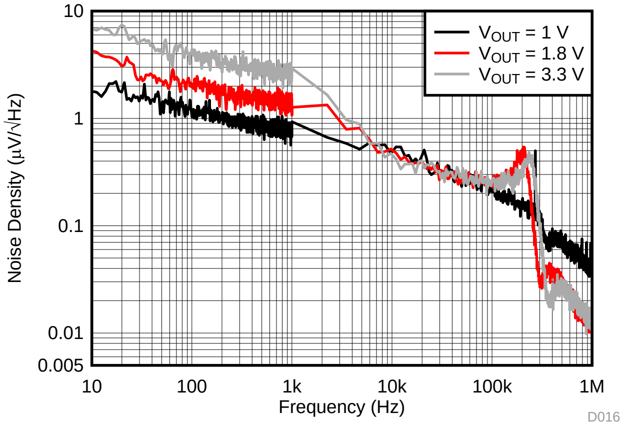
TLV74333PDBV

Figure 20. 3.3-V Foldback Current Limit vs I_{OUT} and Temperature



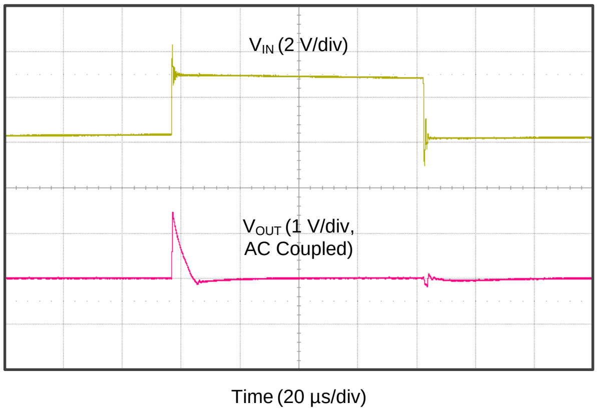
I_{OUT} = 300 mA

Figure 21. Power-Supply Rejection Ratio vs Frequency



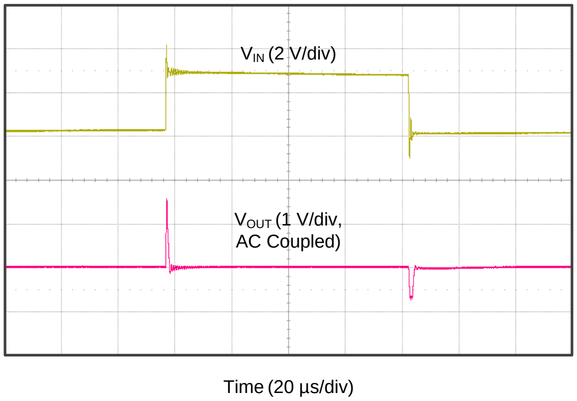
I_{OUT} = 300 mA

Figure 22. Output Spectral Noise Density



TLV74318PDBV, I_{OUT} = 10 mA, 1-µF output capacitor

Figure 23. Line Transient



TLV74318PDBV

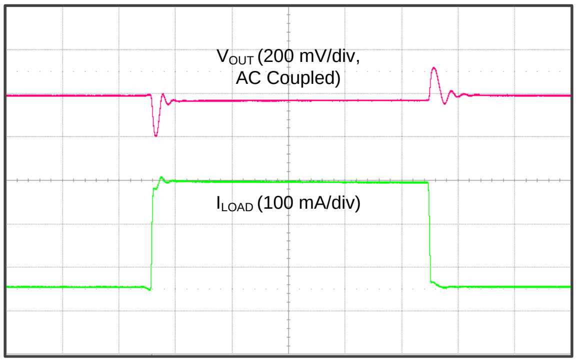
I_{OUT} = 300 mA

1-µF output capacitor

Figure 24. Line Transient

Typical Characteristics (continued)

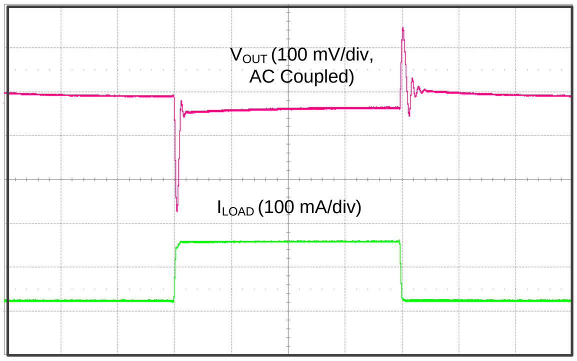
at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



Time (20 µs/div)

TLV74310PDBV V_{IN} = 2 V, 1-µF output capacitor, output current slew rate = 0.25 A/µs

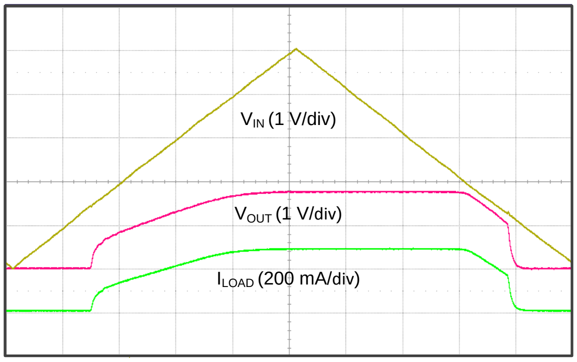
Figure 25. 1-V, 50-mA to 300-mA Load Transient



Time (20 µs/div)

TLV74333PDBV, V_{IN} = 3.8 V,1-µF output capacitor, output current slew rate = 0.25 A/µs

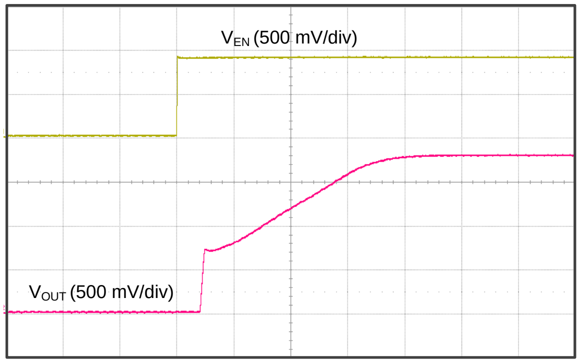
Figure 26. 3.3 V, 50-mA to 300-mA Load Transient



Time (100 µs/div)

TLV74318PDBV, R_L = 6.2 Ω, V_{EN} = V_{IN}, 1-µF output capacitor

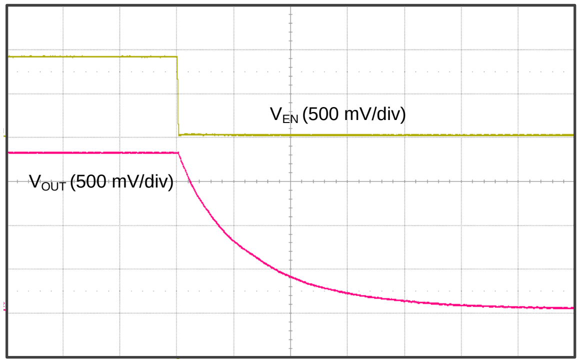
Figure 27. V_{IN} Power-Up and Power-Down



Time (100 µs/div)

TLV74318PDBV, R_L = 6.2 Ω, 1-µF output capacitor

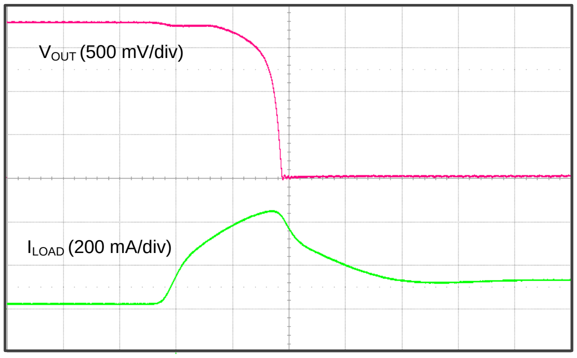
Figure 28. Startup with EN



Time (100 µs/div)

TLV74318PDBV, I_{OUT} = 300 mA, 1-µF output capacitor

Figure 29. Shutdown Response With Enable



Time (100 µs/div)

TLV74318PDBV, 1-µF output capacitor

Figure 30. Foldback Current Limit Response

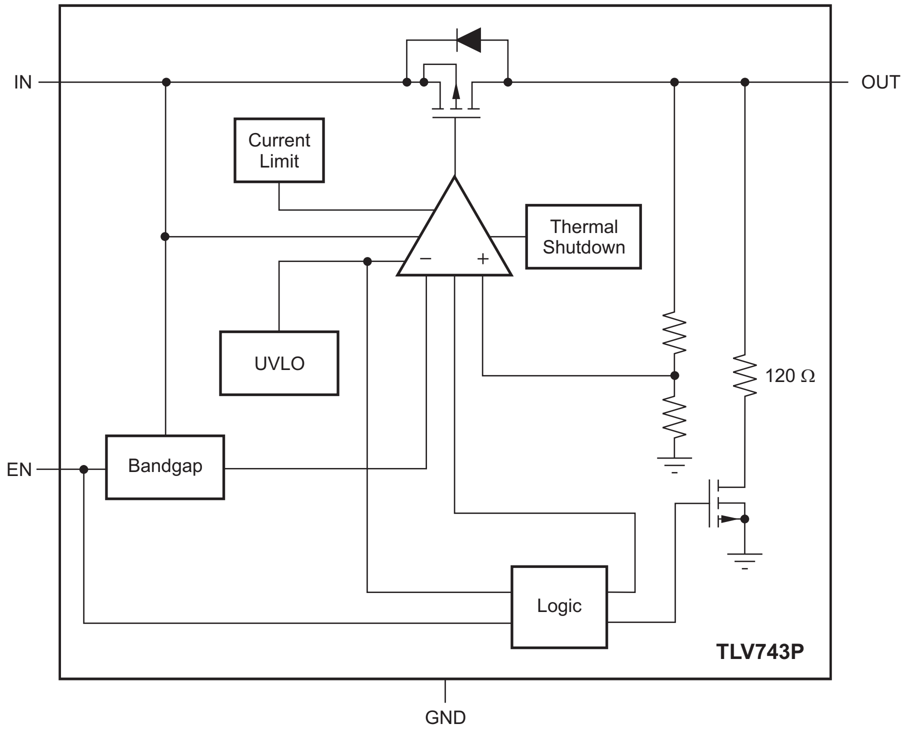
8 Detailed Description

8.1 Overview

The TLV743P device belongs to a new family of next-generation, low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low-dropout voltage, make this device well-suited for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The TLV743P device uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage, $UVLO_{RISE}$. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. During UVLO disable, the output connects to ground with a 120-Ω pulldown resistor.

8.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.35 V. If shutdown capability is not required, connect EN to IN.

The TLV743P device has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in Equation 1:

$$t = \frac{120 \times R_L}{120 + R_L} \times C_{OUT} \tag{1}$$

8.3.3 Internal Foldback Current Limit

The TLV743P device has an internal foldback current limit that protects the regulator during fault conditions. The current allowed through the device is reduced as the output voltage falls. When the output is shorted, the LDO supplies a typical current of 150 mA. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output is shorted, the PMOS pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{OS}]$ until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Information* for more details.

The foldback current limit circuit limits the current allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{LIM}) during startup. See Figure 18 to Figure 20 for typical foldback current limit values. If the output is loaded by a constant-current load during startup, or if the output voltage is negative when the device is enabled, then the required load current by the load may exceed the foldback current limit and the device may not rise to the full output voltage. For constant current loads, disable the output load until the TLV743P has risen to the nominal output voltage.

The TLV743P PMOS pass element has an intrinsic body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. Do not force the output voltage to exceed the input voltage because excessively high current may flow through the body diode.

8.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 160°C. Disabling the device eliminates power dissipated by the device, which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, which protects the device from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{IN} - V_{OUT}$) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV743P internal protection circuitry protects against overload conditions, but is not intended to be active in normal operation. Continuously running the TLV743P device into thermal shutdown degrades device reliability.

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the thermal shutdown temperature.

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

When the device is disabled, the active pulldown resistor discharges the output.

Table 1 lists the conditions that result in different operating modes.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT}(nom) + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT}(nom) + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 160°C$

9 Application and Implementation

9.1 Application Information

9.1.1 Input and Output Capacitor Selection

The TLV743P device uses an advanced internal control loop to obtain stable operation with the use of input or output capacitors. An output capacitance of 1 μF or larger generally provides good dynamic response. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, increased output impedance from the input supply may compromise the performance of the TLV743P. Good analog design practice is to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is greater than 0.5 Ω. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

9.1.2 Dropout Voltage

The TLV743P device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See Figure 7 to Figure 12 for typical dropout values.

Application Information (continued)

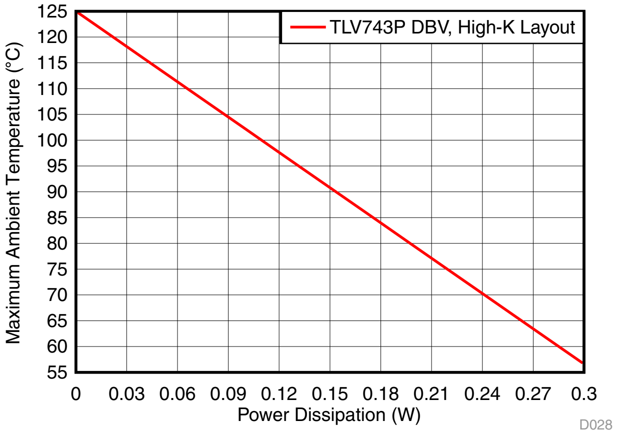
9.1.3 Power Dissipation

The ability to remove heat from the die is different for each package type and presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC high-K boards are shown in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heat sink effectiveness.

Power dissipation (P_D) depends on input voltage and load conditions. P_D is equal to the product of the output current and voltage drop across the output pass element, as shown in Equation 2.

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \tag{2}$$

Figure 31 shows the maximum ambient temperature versus the power dissipation of the TLV743P device in the DQN package. This figure assumes the device is soldered on JEDEC standard high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure that the TLV743P device does not operate continuously above a junction temperature of 125°C.



TLV743P, high-K layout

Figure 31. Maximum Ambient Temperature vs Device Power Dissipation

9.2 Typical Applications

9.2.1 DC-DC Converter Post Regulation

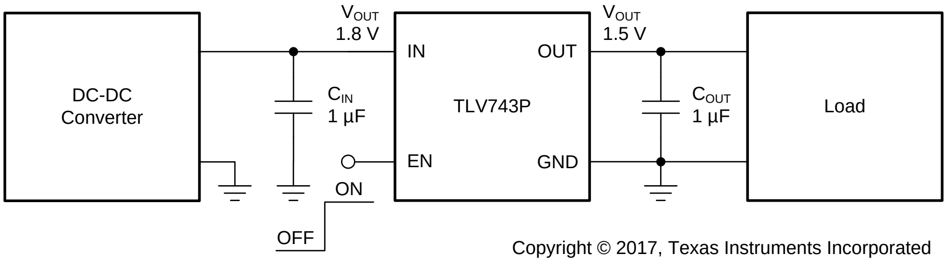


Figure 32. DC-DC Converter Post Regulation

9.2.1.1 Design Requirements

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V, ±5%
Output voltage	1.5 V, ±1%
Output current	200-mA DC, 300-mA peak
Output voltage transient deviation	< 10%, 1-A/µs load step from 50 mA to 200 mA
Maximum ambient temperature	85°C

9.2.1.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 1 µF are selected to give the maximum output capacitance in a small, low-cost package.

Figure 7 shows the 1.2-V option dropout voltage. Given that dropout voltages are higher for lower output-voltage options, and given that the 1.2-V option dropout voltage is typically less than 300 mV at 125°C, then the 1.5-V option dropout voltage is typically less than 300 mV at 125°C.

See Figure 31 to verify that the maximum junction temperature is not exceeded.

9.2.1.3 Application Curve

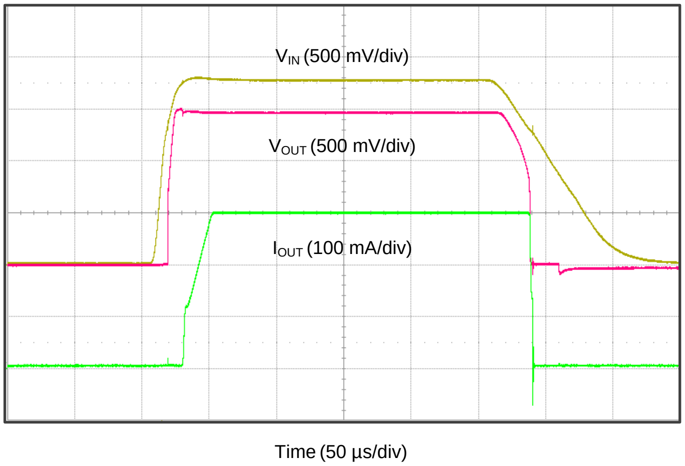


Figure 33. 1.8-V to 1.5-V Regulation at 300 mA

10 Power-Supply Recommendations

Connect a low-output impedance power supply directly to the IN pin of the TLV743P device. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor.

11 Layout

11.1 Layout Guidelines

- Place input and output capacitors as close as possible to the device.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute heat.

11.2 Layout Examples

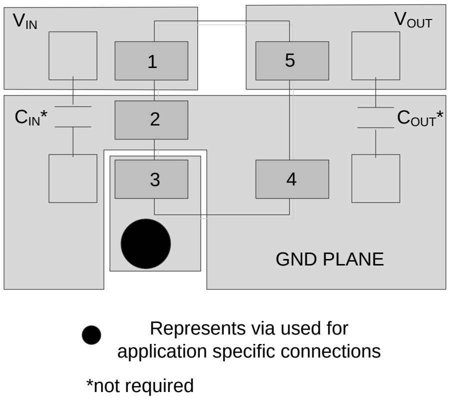


Figure 34. Layout Example: DBV Package

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV743P device. The TLV73312PEVM-643 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

12.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TLV743P**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TLV743 family will actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

(2) Output voltages from 1 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

12.2 Documentation Support

12.2.1 Related Documentation

TLV73312PDQN-643 Evaluation Module User Guide (SBVU024)

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV74310PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
TLV74311PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
TLV74312PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1DBT	Samples
TLV74315PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
TLV74318PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
TLV74325PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
TLV743285PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
TLV74328PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples
TLV74330PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1DGT	Samples
TLV74333PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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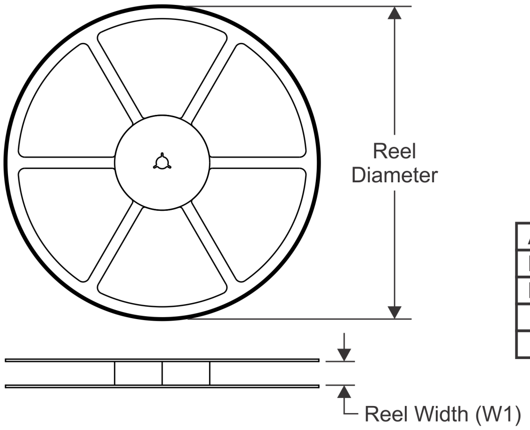
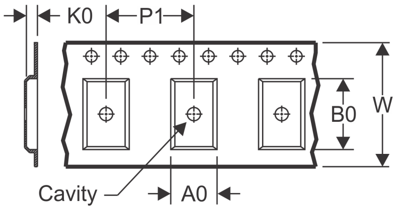
TAPE AND REEL INFORMATION

REEL DIMENSIONS

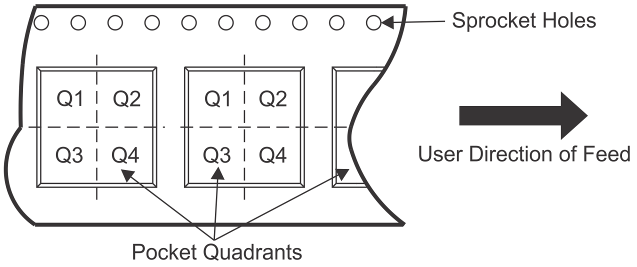


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

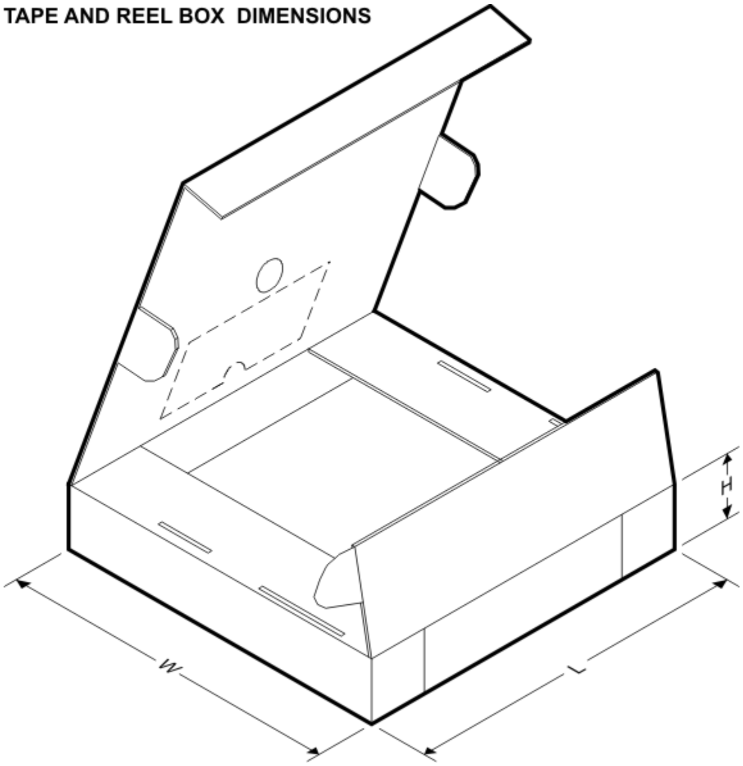
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74310PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74311PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74312PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74315PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74318PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74325PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV743285PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74328PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74330PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74333PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

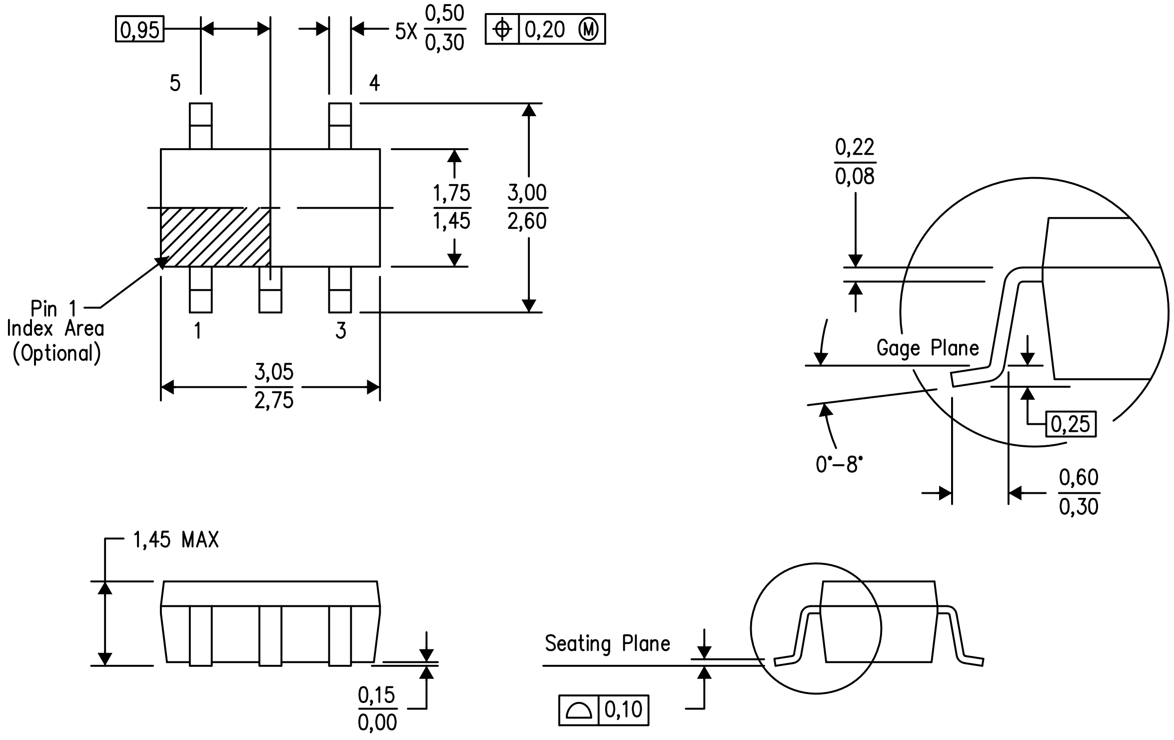
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74310PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74311PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74312PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74315PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74318PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74325PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV743285PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74328PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74330PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74333PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

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