INTEGRATED CIRCUITS
UNITRODE

UC1871
UC2871
UC3871

Resonant Fluorescent Lamp Driver

FEATURES

- 1µA ICC when Disabled
- PWM Control for LCD Supply
- Zero Voltage Switched (ZVS) on Push-Pull Drivers
- Open Lamp Detect Circuitry
- 4.5V to 20V Operation
- Non-saturating Transformer Topology
- Smooth 100% Duty Cycle on Buck PWM and 0% to 95% on Flyback PWM

DESCRIPTION

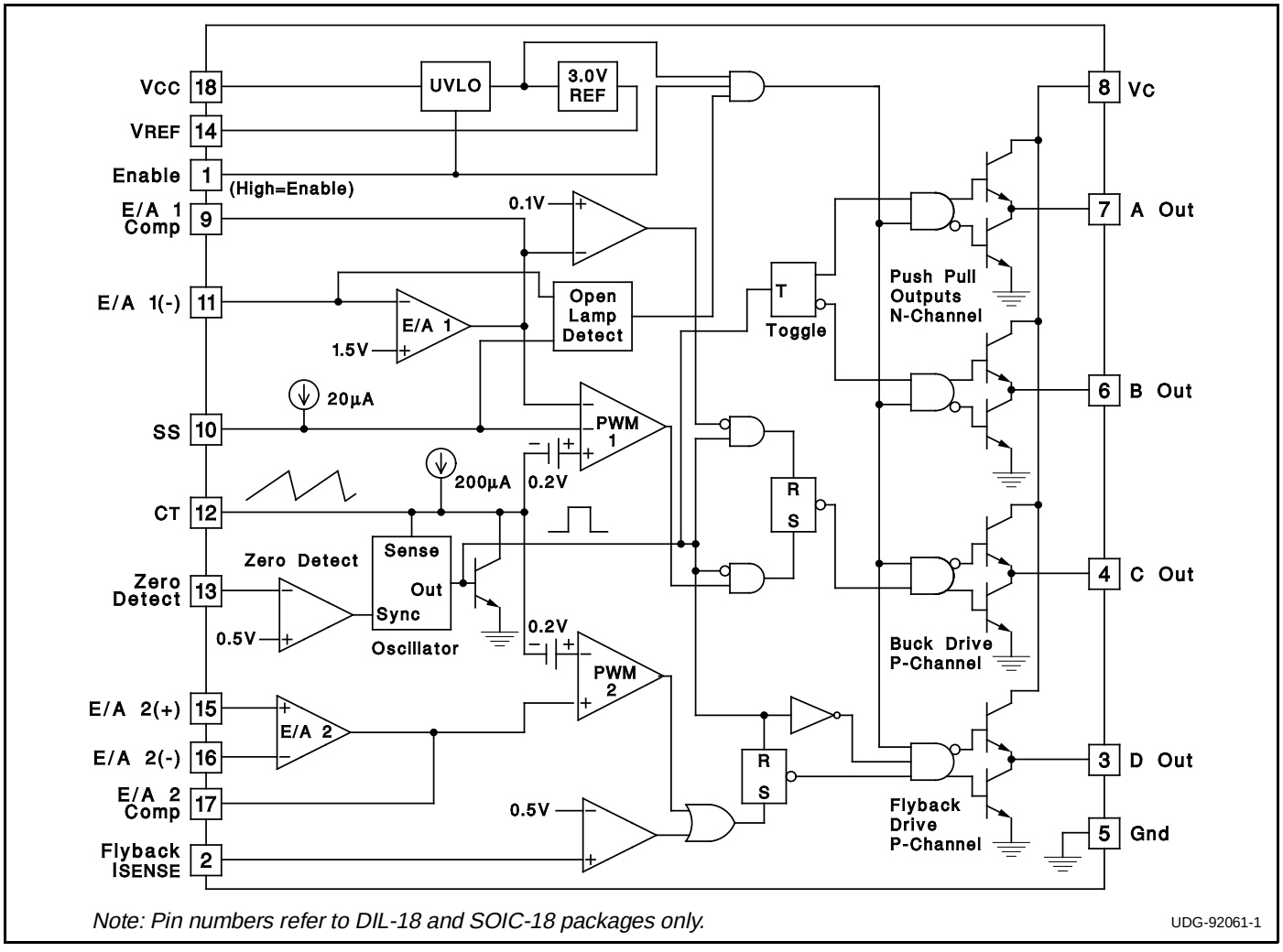
The UC1871 Family of IC's is optimized for highly efficient fluorescent lamp control. An additional PWM controller is integrated on the IC for applications requiring an additional supply, as in LCD displays. When disabled the IC draws only 1µA, providing a true disconnect feature, which is optimum for battery powered systems. The switching frequency of all outputs are synchronized to the resonant frequency of the external passive network, which provides Zero Voltage Switching on the Push-Pull drivers.

Soft-Start and open lamp detect circuitry have been incorporated to minimize component stress. An open lamp is detected on the completion of a soft-start cycle.

The Buck controller is optimized for smooth duty cycle control to 100%, while the flyback control ensures a maximum duty cycle of 95%.

Other features include a precision 1% reference, under voltage lockout, flyback current limit, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



Note: Pin numbers refer to DIL-18 and SOIC-18 packages only.

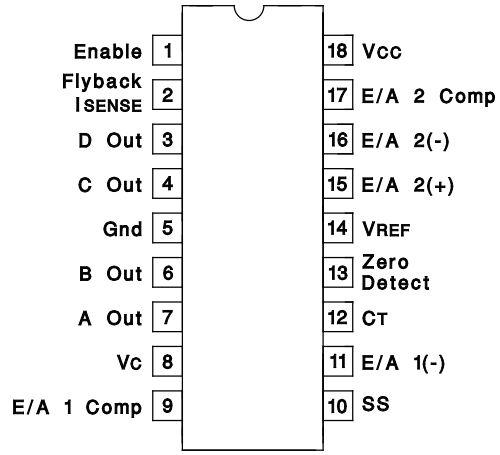
UDG-92061-1

ABSOLUTE MAXIMUM RATINGS

Analog Inputs . . . . . –0.3 to +10V
V_{CC}, V_C Voltage . . . . . +20V
Zero Detect Input Current
  High Impedance Source . . . . . +10mA
Zero Detect
  Low Impedance Source. . . . . +20V
Power Dissipation at T_A = 25°C 1W
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature . . . . . 300°C

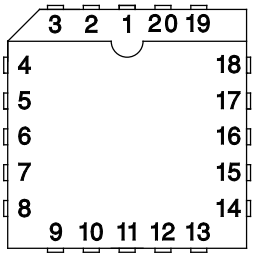
Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



CONNECTION DIAGRAMS

PLCC-20 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
Gnd	1
B Out	2
A Out	3
V_C	4
E/A 1 Comp	5
SS	6
E/A 1(-)	7
N/C	8
C_T	9
Zero Detect	10
N/C	11
V_{REF}	12
E/A 2(+)	13
E/A 2(-)	14
E/A 2 Comp	15
V_{CC}	16
Enable	17
Flyback I_{SENSE}	18
D Out	19
C Out	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_A = -55°C to +125°C for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; V_{CC} = 5V, V_C = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J=25°C	2.963	3.000	3.037	V
	Overtemp	2.940	3.000	3.060	V
Line Regulation	V_{CC} = 4.75V to 18V			10	mV
Load Regulation	Io=0 to -5mA			10	mV
Oscillator Section					
Free Running Freq	T_J=25°C	57	68	78	kHz
Max Sync Frequency	T_J=25°C	160	200	240	kHz
Charge Current	V_{CT} = 1.5V	180	200	220	µA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp 1 Section					
Input Voltage	V_O = 2V	1.445	1.475	1.505	V
Input Bias Current			-0.4	-2	µA
Open Loop Gain	V_O = 0.5 to 3V	65	90		dB
Output High	V_{EA}(-) = 1.3V	3.1	3.5	3.9	V
Output Low	V_{EA}(-) = 1.7V		0.1	0.2	V
Output Source Current	V_{EA}(-) = 1.3V, Vo = 2V	-350	-500		µA
Output Sink Current	V_{EA}(-) = 1.7V, Vo = 2V	10	20		mA
Common Mode Range		0		V_{IN}-1V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Maximum Source Impedance	Note 5			100k	Ω

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these parameters apply for T_A = -55°C to +125°C for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; V_{CC} = 5V, V_C = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Lamp Detect Section					
Soft Start Threshold	V_{EA}(-) = 0V	2.9	3.4	3.8	V
Error Amp Threshold	V_{SS} = 4.2V	0.7	1.0	1.3	V
Soft Start Current	V_{SS} = 2V	10	20	40	µA
Error Amp 2 Section					
Input Offset Voltage	V_O = 2V		0	10	mV
Input Bias Current			-0.2	-1	µA
Input Offset Current				0.5	µA
Open Loop Gain	V_O = 0.5 to 3V	65	90		dB
Output High	V_{ID} = 100mV, V_O = 2V	3.6	4	4.4	V
Output Low	V_{ID} = -100mv, V_O = 2V		0.1	0.2	V
Output Source Current	V_{ID} = 100mV, V_O = 2V	-350	-500		µA
Output Sink Current	V_{ID} = -100mV, V_O = 2V	10	20		mA
Common Mode Range		0		V_{IN}-2V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Isense Section					
Threshold		0.475	0.525	0.575	V
Output Section					
Output Low Level	I_{OUT} = 0, Outputs A and B		0.05	0.2	V
	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Output High Level	I_{OUT} = 0, Outputs C and D	14.7	14.9		V
	I_{OUT} = -10mA	13.5	14.3		V
	I_{OUT} = -100mA	12.5	13.5		V
Rise Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Fall Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	V_{EA}1(-) = 1V	100			%
Out C Min Duty Cycle	V_{EA}1(-) = 2V			0	%
Out D Max Duty Cycle	V_{EA}2(+)- V_{EA}2(-) = 100mV		92	96	%
Out D Min Duty Cycle	V_{EA}2(+)- V_{EA}2(-) = -100mV			0	%
Under Voltage Lockout Section					
Start-Up Threshold		3.7	4.2	4.5	V
Hysterisis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	V_{ENABLE} = 5V		150	400	µA
Supply Current Section					
VCC Supply Current	V_{CC} = 20V		8	14	mA
VC Supply Current	V_C=20V		7	12	mA
ICC Disabled	V_{CC} = 20V, V_{ENABLE} = 0V		1	10	µA

Note 3: Unless otherwise specified, all voltages are with respect to ground.
Currents are positive into, and negative out of the specified terminal.
Note 4: Guaranteed by design but not 100% tested in production.
Note 5: Impedance below specified maximum guarantees proper operation of the Open Lamp Detect.

TYPICAL APPLICATION

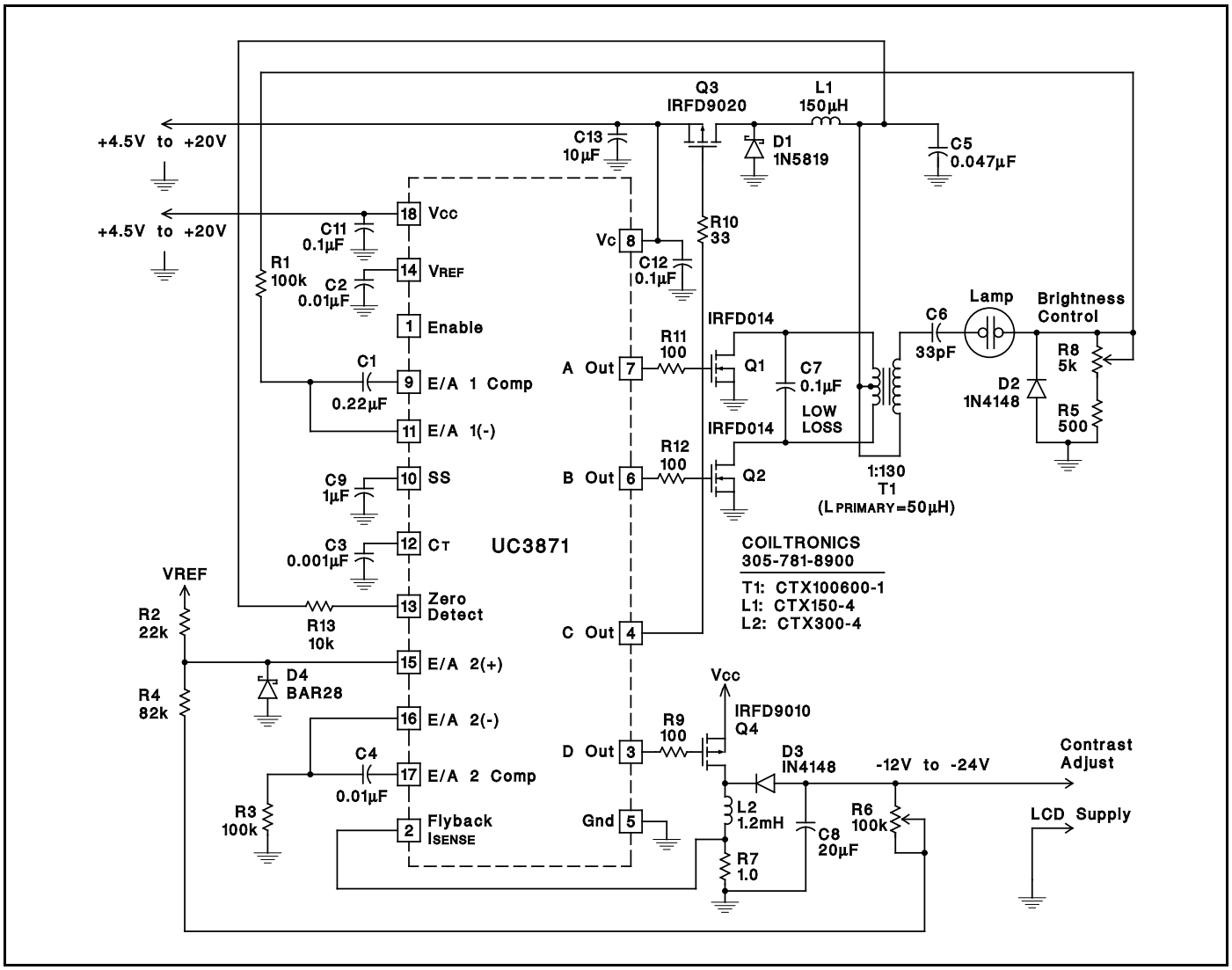


Figure 1

APPLICATION INFORMATION

Figure 1 shows a complete application circuit using the UC3871 Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

APPLICATION INFORMATION (cont.)

UC3871 Oscillator Section

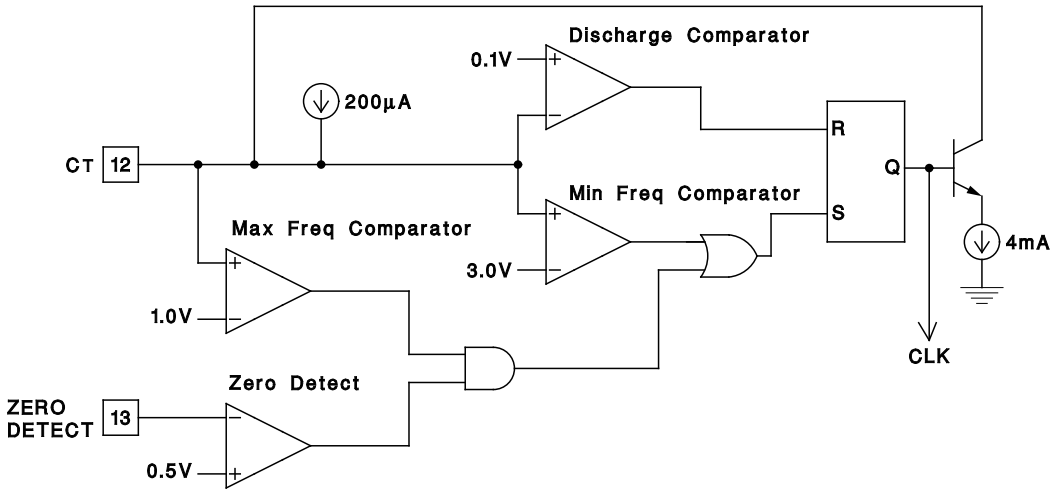


Figure 2

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shutdown, the IC typically draws less than 1µA. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-by-cycle current limiting for added protection.

UC1871 Open Lamp Detect Circuitry

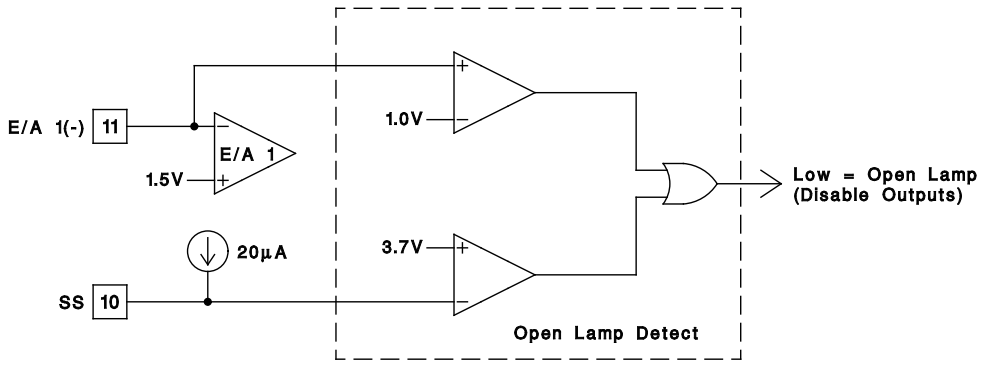


Figure 3

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2871DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2871DW	Samples
UC2871DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2871DW	Samples
UC3871DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3871DW	Samples
UC3871DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3871DW	Samples
UC3871DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3871DW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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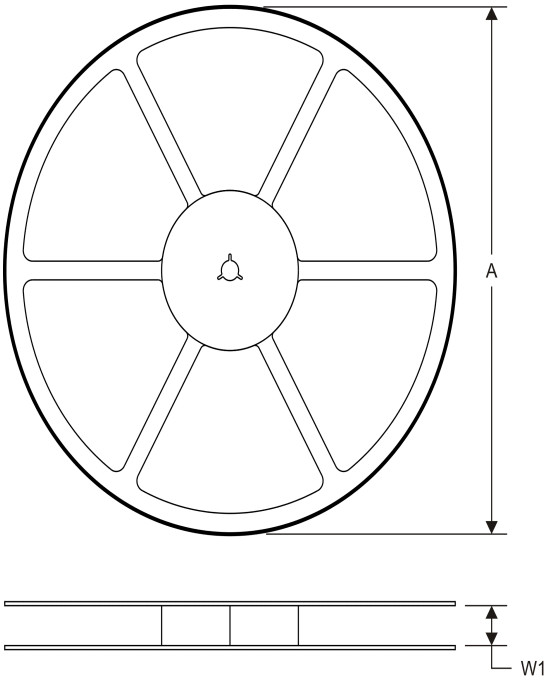
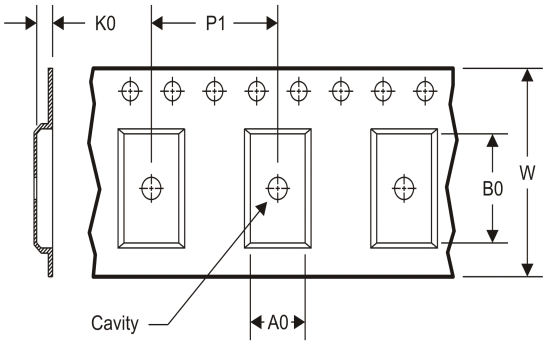
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



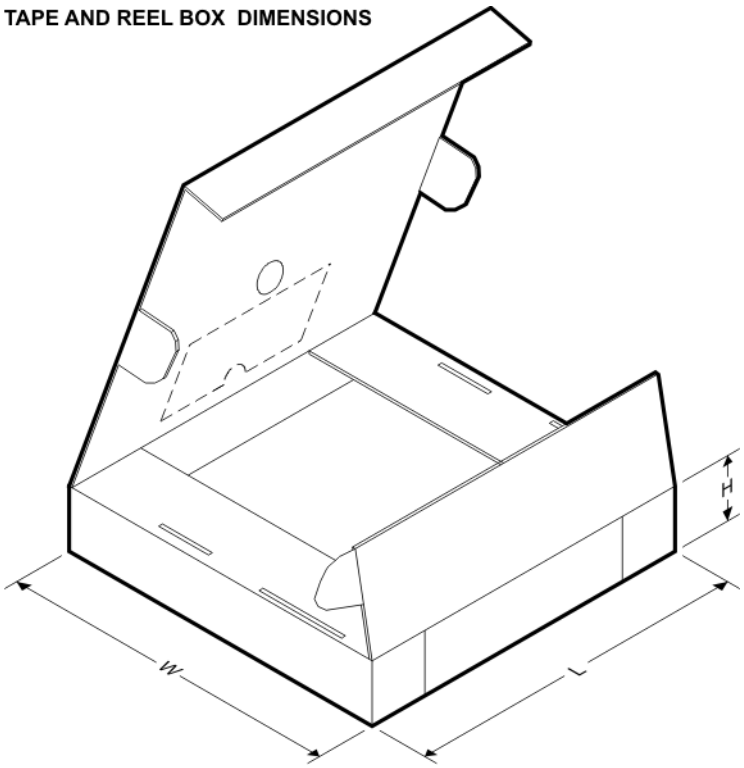
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3871DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

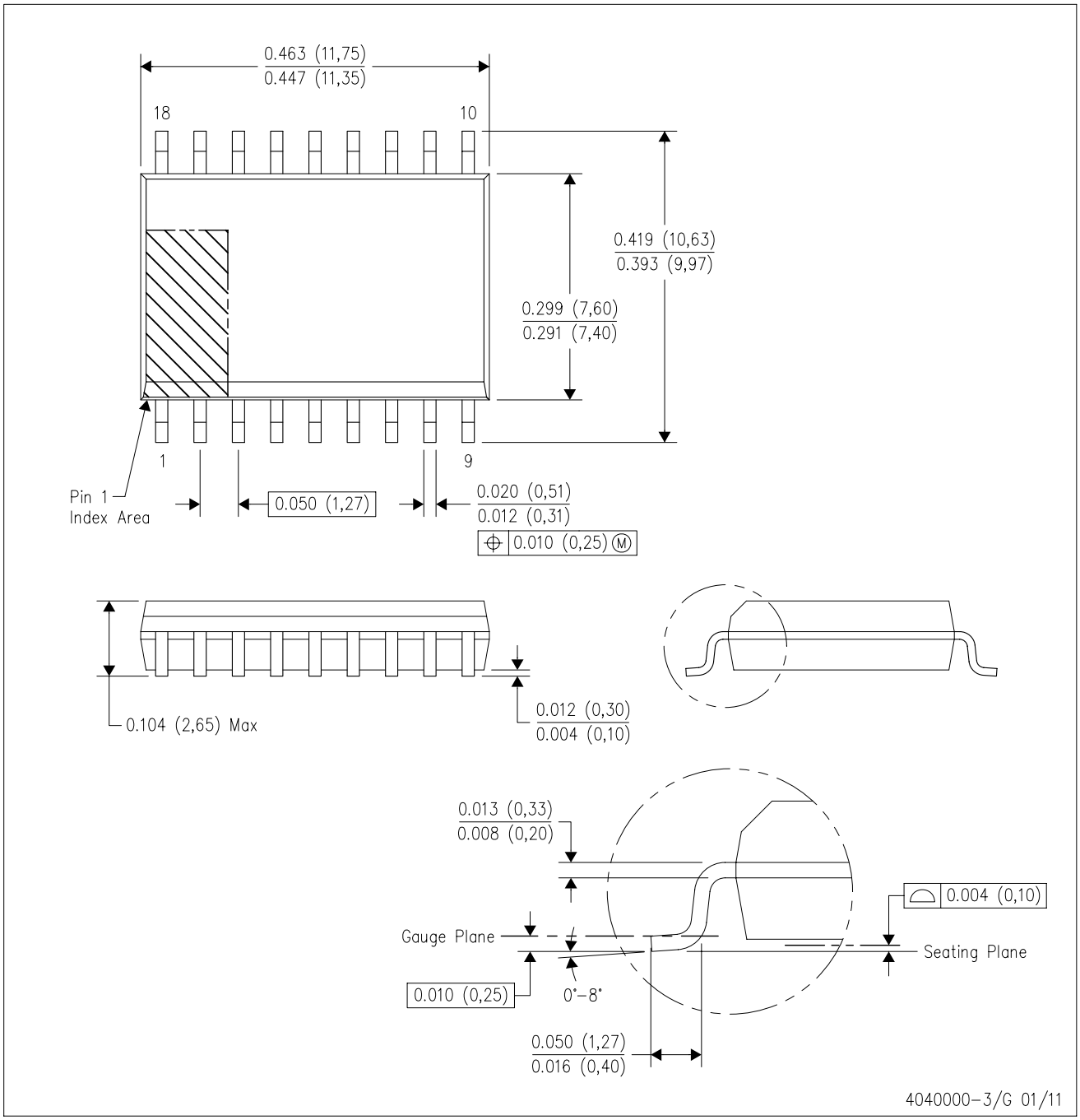
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

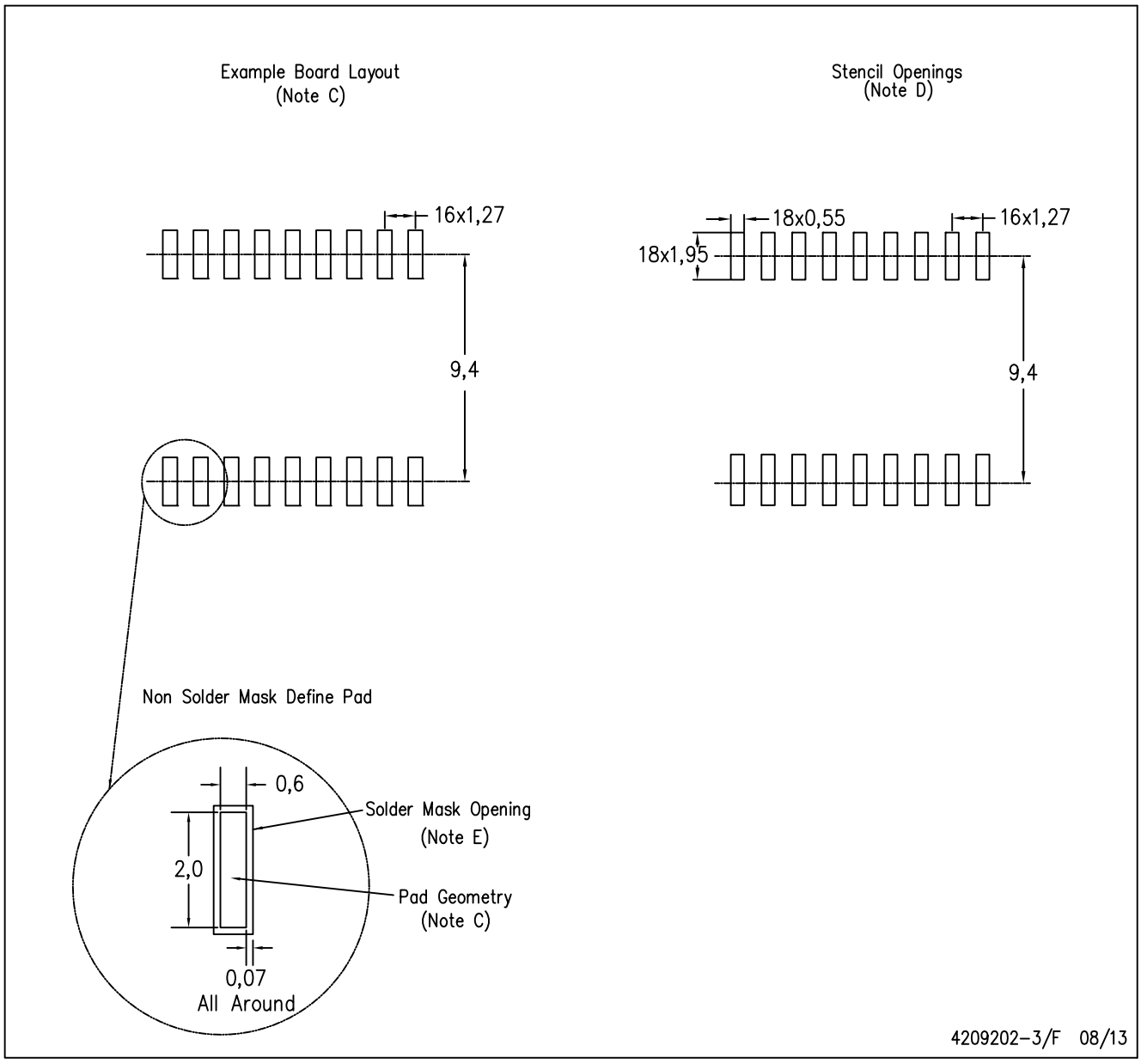
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3871DWTR	SOIC	DW	18	2000	367.0	367.0	45.0

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AB.

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.