

EMIPAK-2B PressFit Power Module 3-Levels Half-Bridge Inverter Stage, 150 A



EMIPAK-2B
(package example)

FEATURES

- Trench IGBT technology
- FRED Pt® clamping diodes
- PressFit pins technology
- Exposed Al₂O₃ substrate with low thermal resistance
- Short circuit rated
- Square RBSOA
- Integrated thermistor
- Low internal inductances
- Low switching loss
- PressFit pins locking technology. Patent # US.263.820 B2
- UL approved file E78996
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

PRODUCT SUMMARY

Q1 - Q4 IGBT STAGE	
V_{CES}	650 V
$V_{CE(ON)}$ typical at $I_C = 100$ A	1.72 V
Q2 - Q3 IGBT STAGE	
V_{CES}	650 V
$V_{CE(ON)}$ typical at $I_C = 150$ A	1.75 V
I_C at $T_C = 82$ °C	150 A
Speed	8 kHz to 30 kHz
Package	EMIPAK-2B
Circuit	3-levels half bridge inverter stage

DESCRIPTION

VS-ETF150Y65U is an integrated solution for a multi level inverter stage in a single package. The EMIPAK-2B package is easy to use thanks to the PressFit pins and the exposed substrate provides improved thermal performance. The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T_J		175	°C
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	$T_J = 25$ °C, all terminals shorted, $f = 50$ Hz, $t = 1$ s	3500	V
Q1 - Q4 IGBT				
Collector to emitter voltage	V_{CES}		650	V
Gate to emitter voltage	V_{GES}		20	
Pulsed collector current	I_{CM}		220	A
Clamped inductive load current	$I_{LM}^{(1)}$		220	
Continuous collector current	I_C	$T_C = 25$ °C	142	A
		$T_C = 60$ °C	121	
		$T_{SINK} = 60$ °C	64	
Power dissipation	P_D	$T_C = 25$ °C	417	W
		$T_C = 60$ °C	319	

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and International patents.



ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Q2 - Q3 IGBT				
Collector to emitter voltage	V_{CES}		650	V
Gate to emitter voltage	V_{GES}		20	
Pulsed collector current	I_{CM}		300	A
Clamped inductive load current	$I_{LM}^{(1)}$		300	
Continuous collector current	I_C	$T_C = 25\text{ }^\circ\text{C}$	201	A
		$T_C = 60\text{ }^\circ\text{C}$	171	
		$T_{SINK} = 60\text{ }^\circ\text{C}$	77	
Power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	600	W
		$T_C = 60\text{ }^\circ\text{C}$	460	
D5 - D6 CLAMPING DIODE				
Repetitive peak reverse voltage	V_{RRM}		650	V
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, $T_J = 25\text{ }^\circ\text{C}$	380	A
Diode continuous forward current	I_F	$T_C = 25\text{ }^\circ\text{C}$	95	
		$T_C = 60\text{ }^\circ\text{C}$	80	
		$T_{SINK} = 60\text{ }^\circ\text{C}$	45	
Power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	221	W
		$T_C = 60\text{ }^\circ\text{C}$	169	
D1 - D2 - D3 - D4 AP DIODE				
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, $T_J = 25\text{ }^\circ\text{C}$	250	A
Diode continuous forward current	I_F	$T_C = 25\text{ }^\circ\text{C}$	78	
		$T_C = 60\text{ }^\circ\text{C}$	66	
		$T_{SINK} = 60\text{ }^\circ\text{C}$	43	
Power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	176	W
		$T_C = 60\text{ }^\circ\text{C}$	135	

Notes

- Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur.
- (1) $V_{CC} = 325\text{ V}$, $V_{GE} = 15\text{ V}$, $L = 500\text{ }\mu\text{H}$, $R_g = 4.7\text{ }\Omega$, $T_J = 175\text{ }^\circ\text{C}$

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Q1 - Q4 IGBT						
Collector to emitter breakdown voltage	BV_{CES}	$V_{GE} = 0\text{ V}$, $I_C = 100\text{ }\mu\text{A}$	650	-	-	V
Collector to emitter voltage	$V_{CE(ON)}$	$V_{GE} = 15\text{ V}$, $I_C = 100\text{ A}$	-	1.72	2.06	
		$V_{GE} = 15\text{ V}$, $I_C = 100\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	1.94	-	
Gate threshold voltage	$V_{GE(th)}$	$V_{CE} = V_{GE}$, $I_C = 3.3\text{ mA}$	5.0	6.3	8.4	
Temperature coefficient of threshold voltage	$\Delta V_{GE(th)}/\Delta T_J$	$V_{CE} = V_{GE}$, $I_C = 1\text{ mA}$ ($25\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$)	-	-19	-	mV/ $^\circ\text{C}$
Forward transconductance	g_{fe}	$V_{CE} = 20\text{ V}$, $I_C = 100\text{ A}$	-	71	-	S
Transfer characteristics	V_{GE}	$V_{CE} = 20\text{ V}$, $I_C = 100\text{ A}$	-	10.5	-	V
Zero gate voltage collector current	I_{CES}	$V_{GE} = 0\text{ V}$, $V_{CE} = 650\text{ V}$	-	0.2	100	μA
		$V_{GE} = 0\text{ V}$, $V_{CE} = 650\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	60	-	
Gate to emitter leakage current	I_{GES}	$V_{GE} = \pm 20\text{ V}$, $V_{CE} = 0\text{ V}$	-	-	± 600	nA



ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Q2 - Q3 IGBT						
Collector to emitter breakdown voltage	BV_{CES}	$V_{GE} = 0\text{ V}, I_C = 100\text{ }\mu\text{A}$	650	-	-	V
Collector to emitter voltage	$V_{CE(ON)}$	$V_{GE} = 15\text{ V}, I_C = 150\text{ A}$	-	1.75	2.17	
		$V_{GE} = 15\text{ V}, I_C = 150\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	1.99	-	
Gate threshold voltage	$V_{GE(th)}$	$V_{CE} = V_{GE}, I_C = 5.0\text{ mA}$	5.0	5.9	8.4	
Temperature coefficient of threshold voltage	$\Delta V_{GE(th)}/\Delta T_J$	$V_{CE} = V_{GE}, I_C = 1.0\text{ mA}$ ($25\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$)	-	-19	-	mV/°C
Forward transconductance	g_{fe}	$V_{CE} = 20\text{ V}, I_C = 150\text{ A}$	-	102	-	S
Transfer characteristics	V_{GE}	$V_{CE} = 20\text{ V}, I_C = 150\text{ A}$	-	9.8	-	V
Zero gate voltage collector current	I_{CES}	$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}$	-	0.2	100	μA
		$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	100	-	
Gate to emitter leakage current	I_{GES}	$V_{GE} = \pm 20\text{ V}, V_{CE} = 0\text{ V}$	-	-	± 600	nA
D5 - D6 CLAMPING DIODE						
Cathode to anode blocking voltage	V_{BR}	$I_R = 100\text{ }\mu\text{A}$	650	-	-	V
Forward voltage drop	V_{FM}	$I_F = 100\text{ A}$	-	2.3	3.15	
		$I_F = 100\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	1.6	-	
Reverse leakage current	I_{RM}	$V_R = 650\text{ V}$	-	0.2	75	μA
		$V_R = 650\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	110	-	
D1 - D2 - D3 - D4 AP DIODE						
Forward voltage drop	V_{FM}	$I_F = 100\text{ A}$	-	2.14	3.18	V
		$I_F = 100\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	1.79	-	

SWITCHING CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Q1 - Q4 IGBT (WITH D5 - D6 CLAMPING DIODE)							
Total gate charge (turn-on)	Q_g	$I_C = 100\text{ A}$ $V_{CC} = 400\text{ V}$ $V_{GE} = 15\text{ V}$	-	190	-	nC	
Gate to emitter charge (turn-on)	Q_{ge}		-	65	-		
Gate to collector charge (turn-on)	Q_{gc}		-	80	-		
Turn-on switching loss	E_{ON}	$I_C = 100\text{ A}$ $V_{CC} = 325\text{ V}$ $V_{GE} = 15\text{ V}$ $R_g = 4.7\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$ ⁽¹⁾	-	0.43	-	mJ	
Turn-off switching loss	E_{OFF}		-	1.04	-		
Total switching loss	E_{TOT}		-	1.47	-		
Turn-on delay time	$t_{d(on)}$		$I_C = 100\text{ A}$ $V_{CC} = 325\text{ V}$ $V_{GE} = 15\text{ V}$ $R_g = 4.7\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$ $T_J = 125\text{ }^\circ\text{C}$ ⁽¹⁾	-	113	-	ns
Rise time	t_r			-	50	-	
Turn-off delay time	$t_{d(off)}$			-	108	-	
Fall time	t_f			-	57	-	
Turn-on switching loss	E_{ON}	-		0.61	-		
Turn-off switching loss	E_{OFF}	$I_C = 100\text{ A}$ $V_{CC} = 325\text{ V}$ $V_{GE} = 15\text{ V}$ $R_g = 4.7\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$ $T_J = 125\text{ }^\circ\text{C}$ ⁽¹⁾	-	1.49	-	mJ	
Total switching loss	E_{TOT}		-	2.1	-		
Turn-on delay time	$t_{d(on)}$		-	113	-		
Rise time	t_r		$I_C = 100\text{ A}$ $V_{CC} = 325\text{ V}$ $V_{GE} = 15\text{ V}$ $R_g = 4.7\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$ $T_J = 125\text{ }^\circ\text{C}$ ⁽¹⁾	-	51	-	ns
Turn-off delay time	$t_{d(off)}$			-	117	-	
Fall time	t_f			-	79	-	
Input capacitance	C_{ies}			$V_{GE} = 0\text{ V}$	-	6600	
Output capacitance	C_{oes}	$V_{CC} = 30\text{ V}$		-	340		
Reverse transfer capacitance	C_{res}	$f = 1\text{ MHz}$	-	180			
Reverse bias safe operating area	RBSOA	$T_J = 175\text{ }^\circ\text{C}, I_C = 220\text{ A}$ $V_{CC} = 325\text{ V}, V_P = 650\text{ V}$ $R_g = 4.7\text{ }\Omega, V_{GE} = 15\text{ V to }0\text{ V}$	Fullsquare				
Short circuit safe operating area	SCSOA	$R_g = 5.0\text{ }\Omega, V_{CC} = 400\text{ V}, V_P = 600\text{ V}$ $V_{GE} = 15\text{ V to }0, T_J = 150\text{ }^\circ\text{C}$	-	-	5.5	μs	



SWITCHING CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Q2 - Q3 IGBT (WITH D2 - D3 AP DIODE)						
Total gate charge (turn-on)	Q_g	$I_C = 150\text{ A}$ $V_{CC} = 400\text{ V}$ $V_{GE} = 15\text{ V}$	-	310	-	nC
Gate to emitter charge (turn-on)	Q_{ge}		-	95	-	
Gate to collector charge (turn-on)	Q_{gc}		-	130	-	
Turn-on switching loss	E_{ON}	$I_C = 150\text{ A}$ $V_{CC} = 325\text{ V}$ $V_{GE} = 15\text{ V}$ $R_g = 4.7\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$ ⁽¹⁾	-	0.49	-	mJ
Turn-off switching loss	E_{OFF}		-	2.51	-	
Total switching loss	E_{TOT}		-	3.0	-	
Turn-on delay time	$t_{d(on)}$		-	162	-	ns
Rise time	t_r		-	71	-	
Turn-off delay time	$t_{d(off)}$	-	148	-		
Fall time	t_f	-	64	-		
Turn-on switching loss	E_{ON}	$I_C = 150\text{ A}$ $V_{CC} = 325\text{ V}$ $V_{GE} = 15\text{ V}$ $R_g = 4.7\text{ }\Omega$ $L = 500\text{ }\mu\text{H}$ $T_J = 125\text{ }^\circ\text{C}$ ⁽¹⁾	-	0.62	-	mJ
Turn-off switching loss	E_{OFF}		-	3.18	-	
Total switching loss	E_{TOT}		-	3.8	-	
Turn-on delay time	$t_{d(on)}$		-	162	-	ns
Rise time	t_r		-	75	-	
Turn-off delay time	$t_{d(off)}$	-	153	-		
Fall time	t_f	-	81	-		
Input capacitance	C_{ies}	$V_{GE} = 0\text{ V}$ $V_{CC} = 30\text{ V}$ $f = 1\text{ MHz}$	-	9900	-	pF
Output capacitance	C_{oes}		-	460	-	
Reverse transfer capacitance	C_{res}		-	250	-	
Reverse bias safe operating area	RBSOA	$T_J = 175\text{ }^\circ\text{C}$, $I_C = 300\text{ A}$ $V_{CC} = 325\text{ V}$, $V_P = 650\text{ V}$ $R_g = 4.7\text{ }\Omega$, $V_{GE} = 15\text{ V to } 0\text{ V}$	Fullsquare			
Short circuit safe operating area	SCSOA	$R_g = 5.0\text{ }\Omega$, $V_{CC} = 400\text{ V}$, $V_P = 600\text{ V}$ $V_{GE} = 15\text{ V to } 0$, $T_J = 150\text{ }^\circ\text{C}$	-	-	5.5	μs
D5 - D6 CLAMPING DIODE						
Diode reverse recovery time	t_{rr}	$V_R = 200\text{ V}$ $I_F = 50\text{ A}$ $di/dt = 500\text{ A}/\mu\text{s}$	-	55	-	ns
Diode peak reverse current	I_{rr}		-	8.7	-	A
Diode recovery charge	Q_{rr}		-	242	-	nC
Diode reverse recovery time	t_{rr}	$V_R = 200\text{ V}$ $I_F = 50\text{ A}$ $di/dt = 500\text{ A}/\mu\text{s}$, $T_J = 125\text{ }^\circ\text{C}$	-	112	-	ns
Diode peak reverse current	I_{rr}		-	21	-	A
Diode recovery charge	Q_{rr}		-	1177	-	nC
D1 - D2 - D3 - D4 AP DIODE						
Diode reverse recovery time	t_{rr}	$V_R = 200\text{ V}$ $I_F = 50\text{ A}$ $di/dt = 500\text{ A}/\mu\text{s}$	-	66	-	ns
Diode peak reverse current	I_{rr}		-	11	-	A
Diode recovery charge	Q_{rr}		-	363	-	nC
Diode reverse recovery time	t_{rr}	$V_R = 200\text{ V}$ $I_F = 50\text{ A}$ $di/dt = 500\text{ A}/\mu\text{s}$, $T_J = 125\text{ }^\circ\text{C}$	-	130	-	ns
Diode peak reverse current	I_{rr}		-	21.3	-	A
Diode recovery charge	Q_{rr}		-	1392	-	nC

Note

⁽¹⁾ Energy losses include "tail" and diode reverse recovery.



INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Resistance	R ₂₅	T _C = 25 °C	5000	Ω
	R ₁₀₀	T _C = 100 °C	493 ± 5 %	
B-value	B _{25/50}	R ₂ = R ₂₅ exp. [B _{25/50} (1/T ₂ - 1/(298.15 K))]	3375 ± 5 %	K
Maximum operating temperature			220	°C
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Q1 - Q4 IGBT - Junction to case thermal resistance (per switch)	R _{thJC}	-	-	0.36	°C/W
Q2 - Q3 IGBT - Junction to case thermal resistance (per switch)		-	-	0.25	
D5 - D6 Clamping diode - Junction to case thermal resistance (per diode)		-	-	0.68	
D1 - D2 - D3 - D4 AP diode - Junction to case thermal resistance (per diode)		-	-	0.85	
Q1 - Q4 IGBT - Case to sink thermal resistance (per switch)	R _{thCS} ⁽¹⁾	-	0.63	-	
Q2 - Q3 IGBT - Case to sink thermal resistance (per switch)		-	0.62	-	
D5 - D6 Clamping diode - Case to sink thermal resistance (per diode)		-	1.0	-	
D1 - D2 - D3 - D4 AP diode - Case to sink thermal resistance (per diode)		-	0.78	-	
Case to sink thermal resistance per module		-	0.08	-	°C/W
Mounting torque (M4)		2	-	3	Nm
Weight		-	45	-	g

Note

⁽¹⁾ Mounting surface flat, smooth, and greased

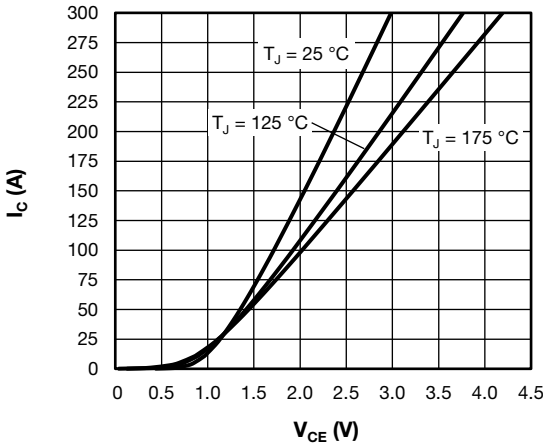


Fig. 1 - I_C vs. V_{CE} , Typical Q1 - Q4 Trench IGBT Output Characteristics, $V_{GE} = 15 V$

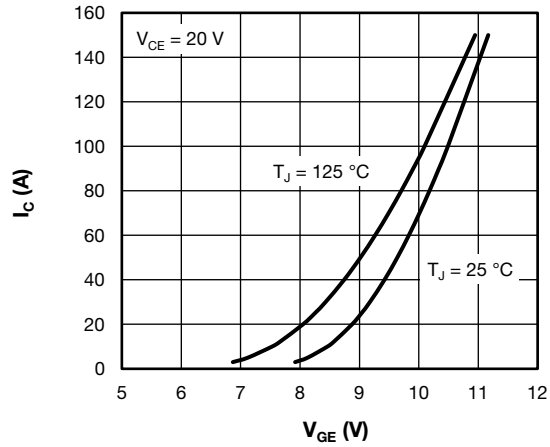


Fig. 4 - I_C vs V_{GE} Typical Q1 - Q4 Trench IGBT Transfer Characteristics

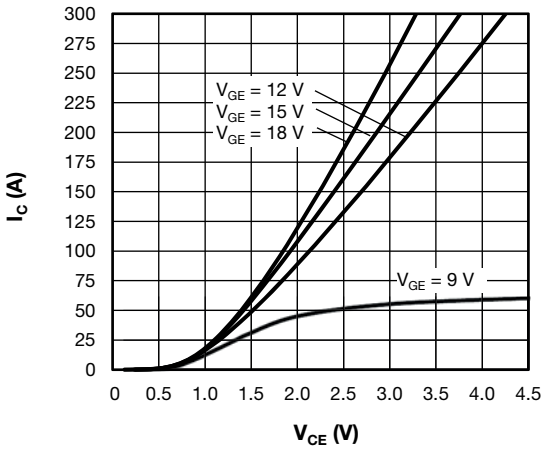


Fig. 2 - I_C vs. V_{CE} Typical Q1 - Q4 Trench IGBT Output Characteristics, $T_J = 125 °C$

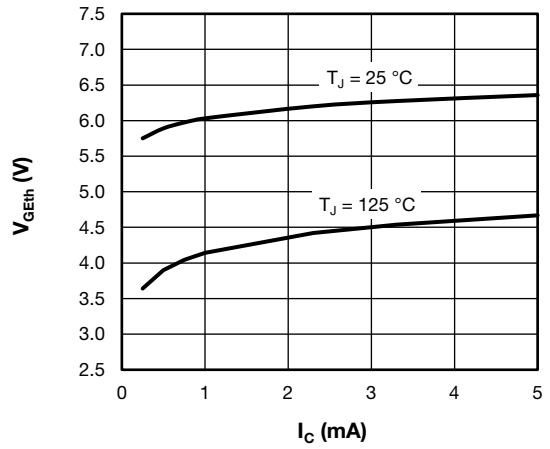


Fig. 5 - V_{Geth} vs. I_C Typical Q1 - Q4 Trench IGBT Gate Threshold Voltage

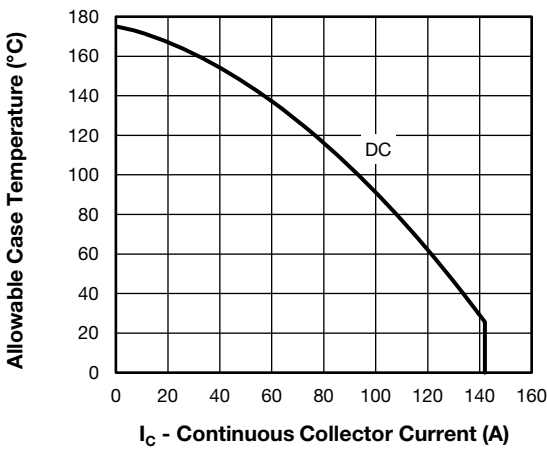


Fig. 3 - Allowable Case Temperature vs. Continuous Collector Current, Maximum Q1 - Q4 IGBT Continuous Collector Current vs. Case Temperature

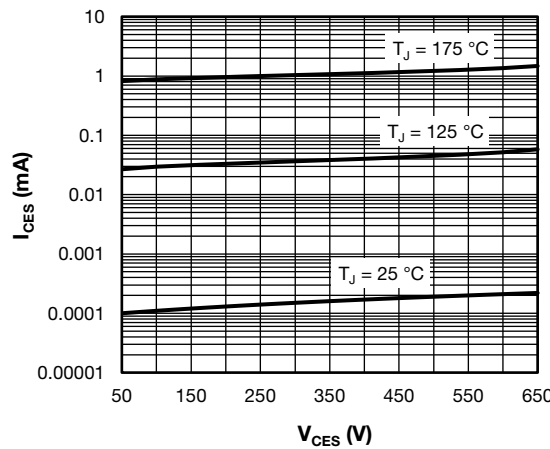


Fig. 6 - I_{CES} vs V_{CES} Typical Q1 - Q4 Trench IGBT Zero Gate Voltage Collector Current

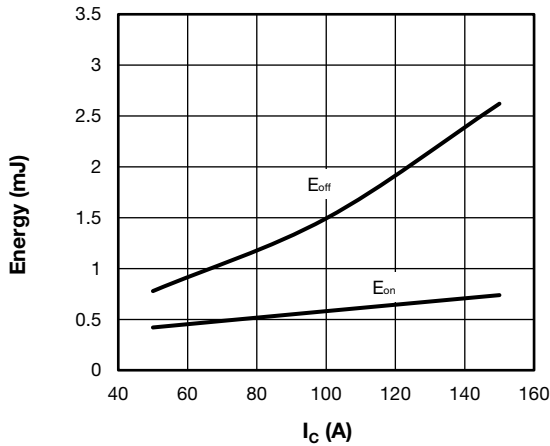


Fig. 7 - Energy Loss vs. I_C
(Typical Q1 - Q4 Trench IGBT Energy Loss vs. I_C (with D5 - D6 Clamping Diode)), $T_J = 125^\circ\text{C}$, $V_{CC} = 325\text{V}$, $R_g = 4.7\ \Omega$, $V_{GE} = \pm 15\text{V}$, $L = 500\ \mu\text{H}$

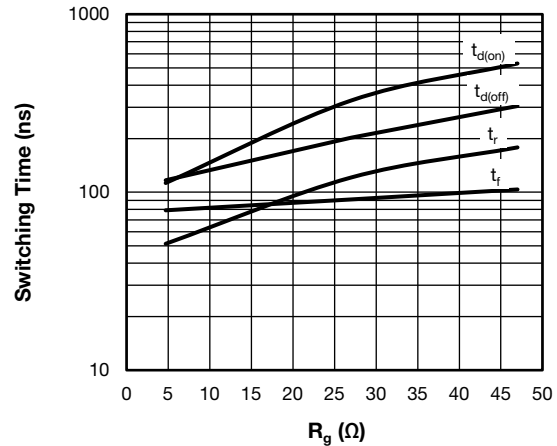


Fig. 10 - Switching Time vs. R_g
(Typical Q1 - Q4 Trench IGBT Switching Time vs. R_g (with D5 - D6 Clamping Diode)), $T_J = 125^\circ\text{C}$, $V_{CC} = 325\text{V}$, $I_C = 100\text{A}$, $V_{GE} = \pm 15\text{V}$, $L = 500\ \mu\text{H}$

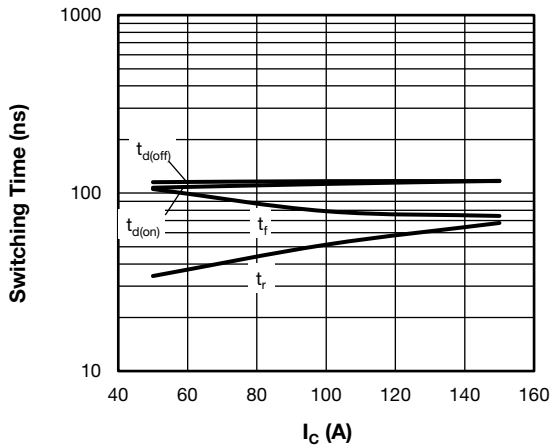


Fig. 8 - Switching Time vs. I_C
(Typical Q1 - Q4 Trench IGBT Switching Time vs. I_C (with D5 - D6 Clamping Diode)), $T_J = 125^\circ\text{C}$, $V_{CC} = 325\text{V}$, $R_g = 4.7\ \Omega$, $V_{GE} = \pm 15\text{V}$, $L = 500\ \mu\text{H}$

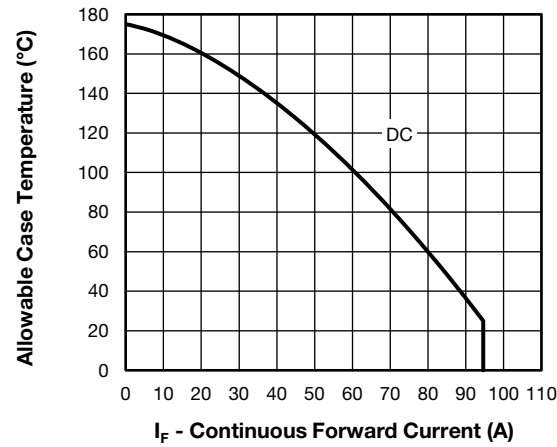


Fig. 11 - Allowable Case Temperature vs. Continuous Collector Current, (Maximum D5 - D6 Diode Continuous Forward Current vs. Case Temperature)

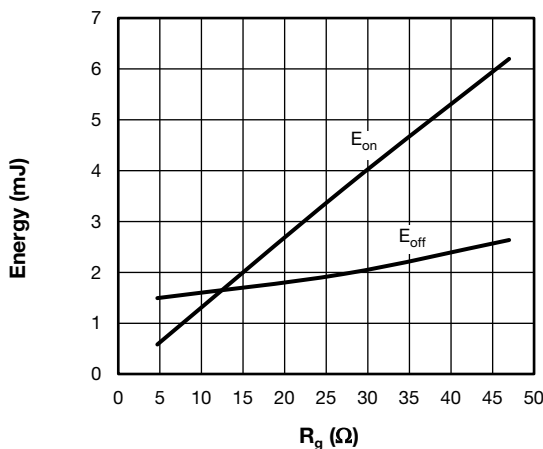


Fig. 9 - Energy Loss vs. R_g
(Typical Q1 - Q4 Trench IGBT Energy Loss vs. R_g (with D5 - D6 Clamping Diode)), $T_J = 125^\circ\text{C}$, $V_{CC} = 325\text{V}$, $I_C = 100\text{A}$, $V_{GE} = \pm 15\text{V}$, $L = 500\ \mu\text{H}$

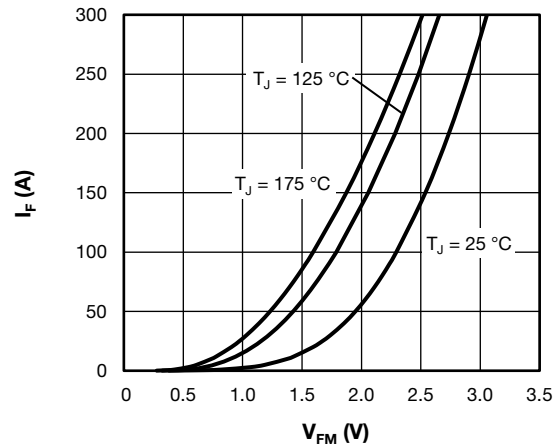


Fig. 12 - I_F vs. V_{FM}
(Typical D5 - D6 Clamping Diode Forward Characteristics)

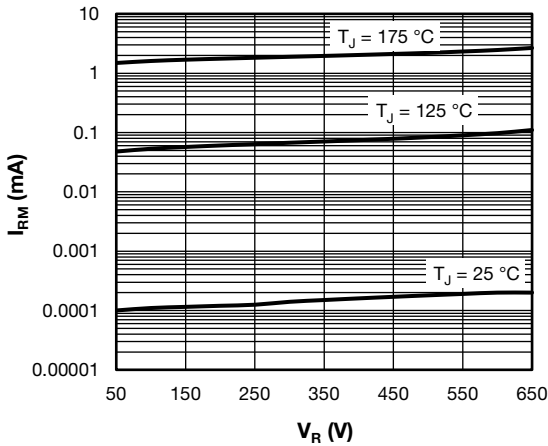


Fig. 13 - I_{RM} vs. V_R
(Typical D5 - D6 Clamping Diode Reverse Leakage Current)

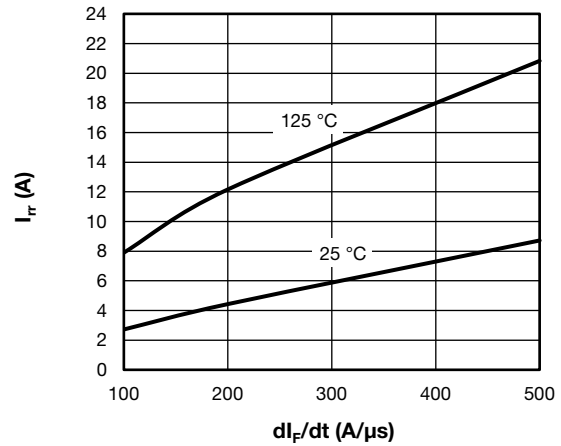


Fig. 15 - I_{rr} vs. di_F/dt
(Typical D5 - D6 Clamping Diode Reverse Recovery Current vs. di_F/dt), $V_{rr} = 200\text{ V}$, $I_F = 50\text{ A}$

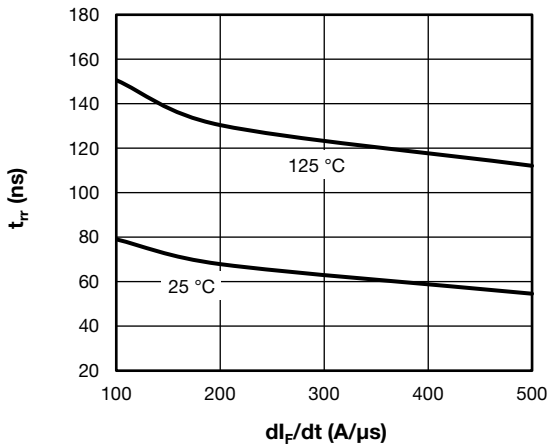


Fig. 14 - t_{rr} vs. di_F/dt
(Typical D5 - D6 Clamping Diode Reverse Recovery Time vs. di_F/dt), $V_{rr} = 200\text{ V}$, $I_F = 50\text{ A}$

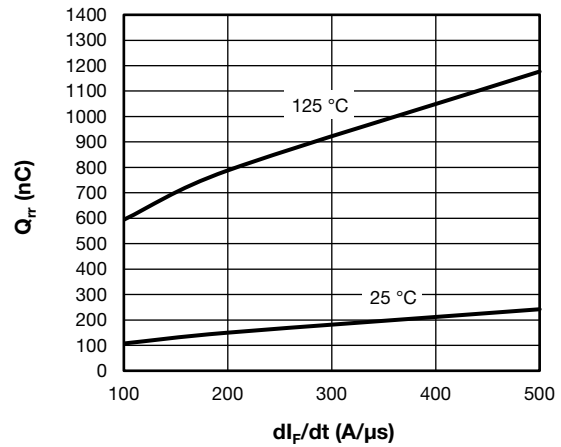


Fig. 16 - Q_{rr} vs. di_F/dt
(Typical D5 - D6 Clamping Diode Reverse Recovery Charge vs. di_F/dt), $V_{rr} = 200\text{ V}$, $I_F = 50\text{ A}$

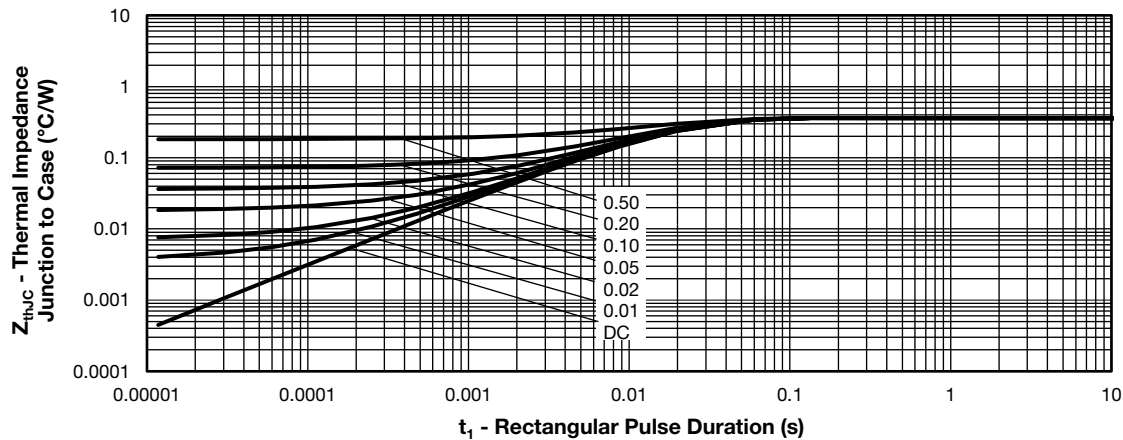


Fig. 17 - Z_{thJC} vs. t_1 Rectangular Pulse Duration (Maximum Thermal Impedance Z_{thJC} Characteristics - (Q1 - Q4 Trench IGBT))

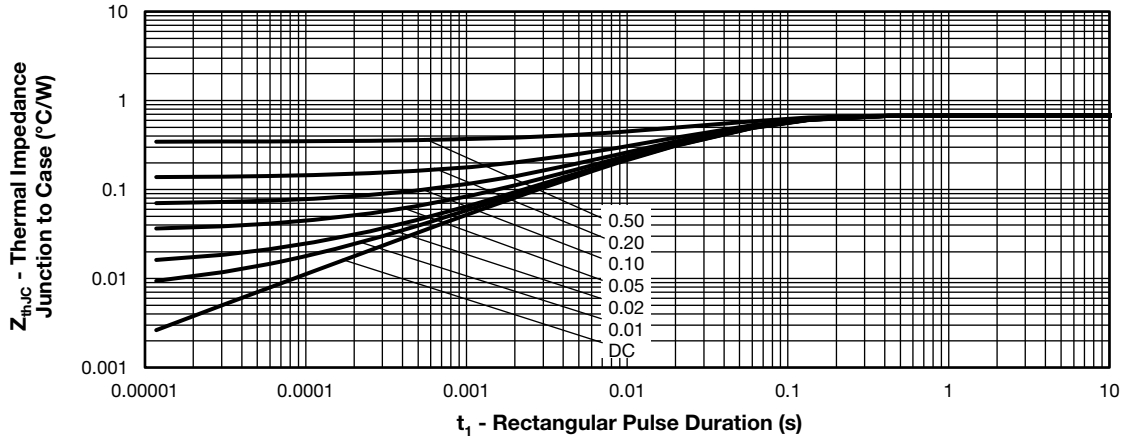


Fig. 18 - Z_{thJC} vs. t_1 Rectangular Pulse Duration (Maximum Thermal Impedance Z_{thJC} Characteristics - (D5 - D6 Clamping Diode))

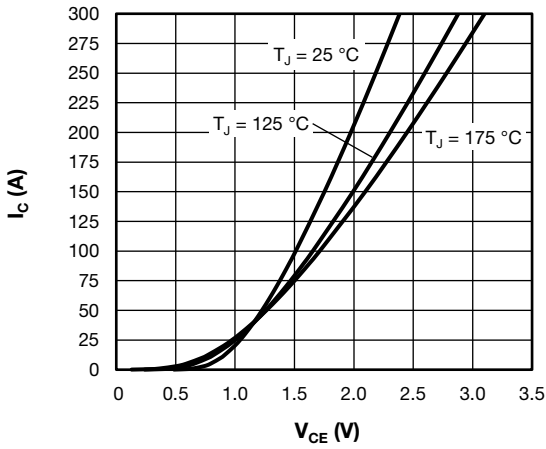


Fig. 19 - I_C vs. V_{CE}
(Typical Q2 - Q3 Trench IGBT Output Characteristics, $V_{GE} = 15$ V)

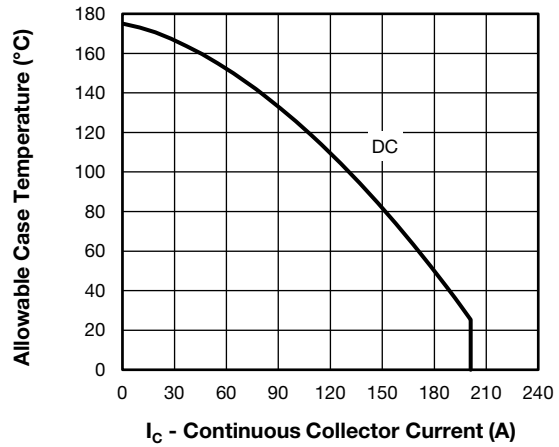


Fig. 21 - Allowable Case Temperature vs. Continuous Collector Current,
(Maximum Q2 - Q3 IGBT Continuous Collector Current vs. Case Temperature)

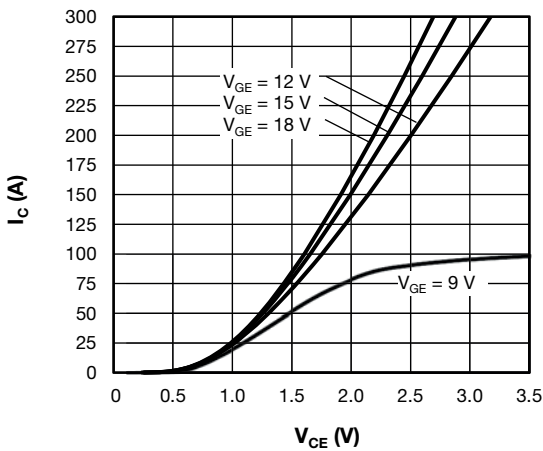


Fig. 20 - I_C vs. V_{CE} (Typical Q2 - Q3 Trench IGBT Output Characteristics, $T_J = 125^\circ\text{C}$)

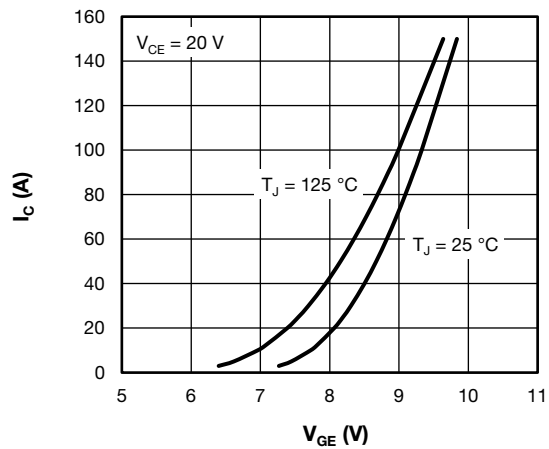


Fig. 22 - I_C vs. V_{GE}
(Typical Q2 - Q3 Trench IGBT Transfer Characteristics)

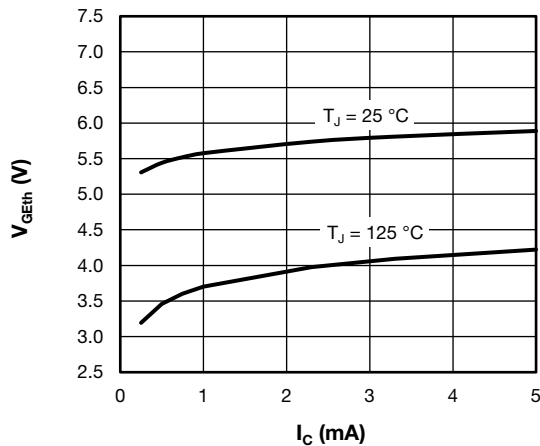


Fig. 23 - V_{GEth} vs. I_C
(Typical Q2 - Q3 Trench IGBT Gate Threshold Voltage)

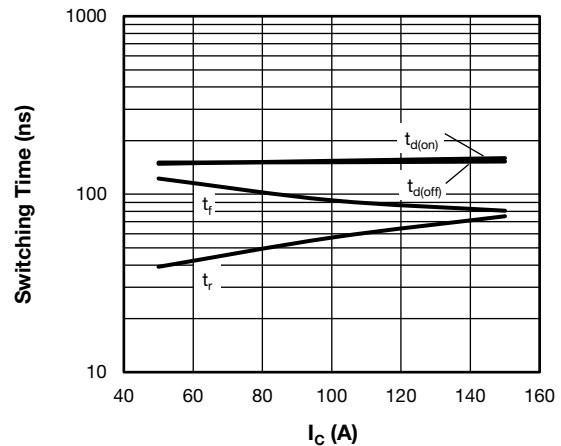


Fig. 26 - Switching Time vs. I_C
(Typical Q2 - Q3 Trench IGBT Switching Time vs. I_C (with D2 - D3 Antiparallel Diode)), $T_J = 125\text{ °C}$, $V_{CC} = 325\text{ V}$, $R_g = 4.7\text{ }\Omega$, $V_{GE} = \pm 15\text{ V}$, $L = 500\text{ }\mu\text{H}$

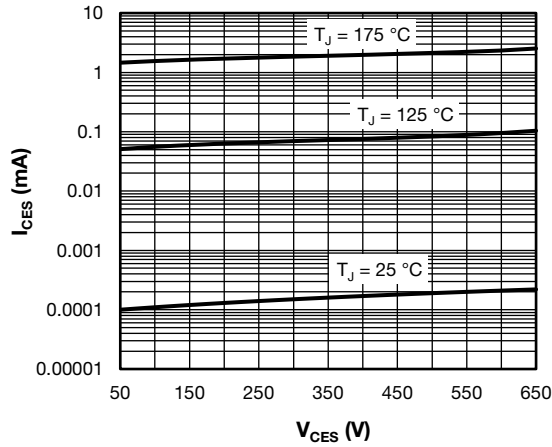


Fig. 24 - I_{CES} vs. V_{CES}
(Typical Q2 - Q3 Trench IGBT Zero Gate Voltage Collector Current)

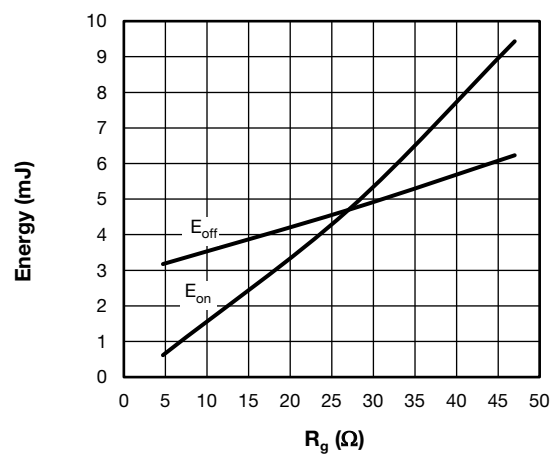


Fig. 27 - Energy Loss vs. R_g
(Typical Q2 - Q3 Trench IGBT Energy Loss vs. R_g (with D2 - D3 Antiparallel Diode)), $T_J = 125\text{ °C}$, $V_{CC} = 325\text{ V}$, $I_C = 150\text{ A}$, $V_{GE} = \pm 15\text{ V}$, $L = 500\text{ }\mu\text{H}$

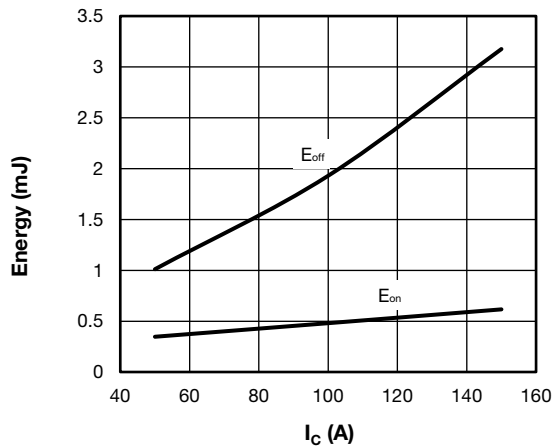


Fig. 25 - Energy Loss vs. I_C
(Typical Q2 - Q3 Trench IGBT Energy Loss vs. I_C (with D2 - D3 Antiparallel Diode)), $T_J = 125\text{ °C}$, $V_{CC} = 325\text{ V}$, $R_g = 4.7\text{ }\Omega$, $V_{GE} = \pm 15\text{ V}$, $L = 500\text{ }\mu\text{H}$

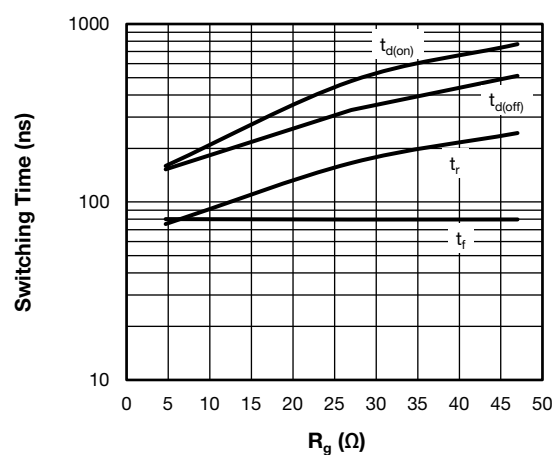


Fig. 28 - Switching Time vs. R_g (Typical Q2 - Q3 Trench IGBT Switching Time vs. R_g (with D2 - D3 Antiparallel Diode)), $T_J = 125\text{ °C}$, $V_{CC} = 325\text{ V}$, $I_C = 150\text{ A}$, $V_{GE} = \pm 15\text{ V}$, $L = 500\text{ }\mu\text{H}$

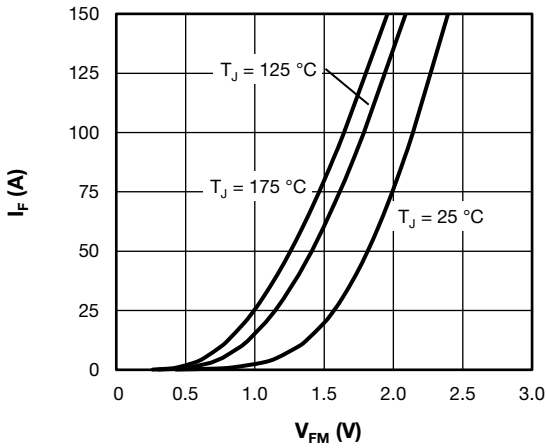


Fig. 29 - I_F vs. V_{FM}
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Forward Characteristics)

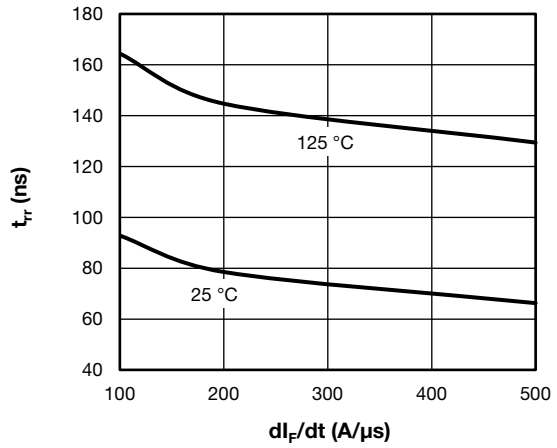


Fig. 31 - t_{rr} vs. di_F/dt
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Reverse Recovery Time vs. di_F/dt), $V_{rr} = 200\text{ V}$, $I_F = 50\text{ A}$

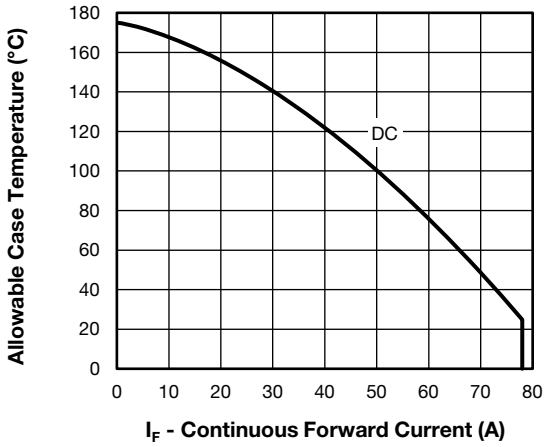


Fig. 30 - Allowable Case Temperature vs. Continuous Collector Current,
(Maximum D1- D2 - D3 - D4 Diode Continuous Forward Current vs. Case Temperature)

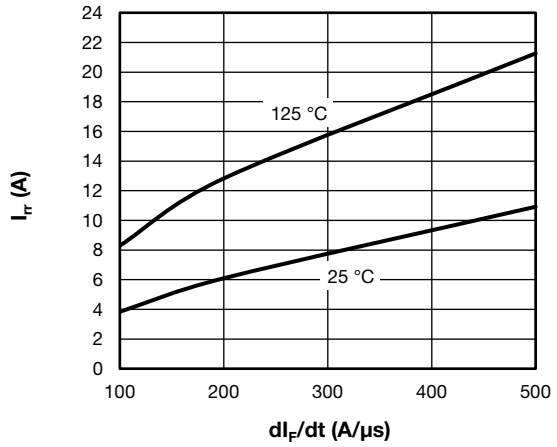


Fig. 32 - I_{rr} vs. di_F/dt
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Reverse Recovery Current vs. di_F/dt), $V_{rr} = 200\text{ V}$, $I_F = 50\text{ A}$

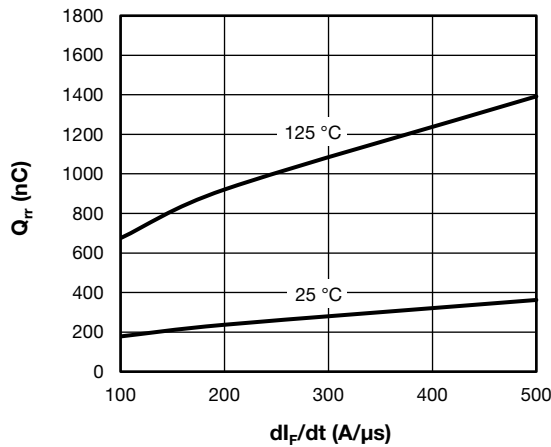


Fig. 33 - Q_{rr} vs. di_F/dt
(Typical D1 - D2 - D3 - D4 Antiparallel Diode Reverse Recovery Charge vs. di_F/dt), $V_{rr} = 200\text{ V}$, $I_F = 50\text{ A}$

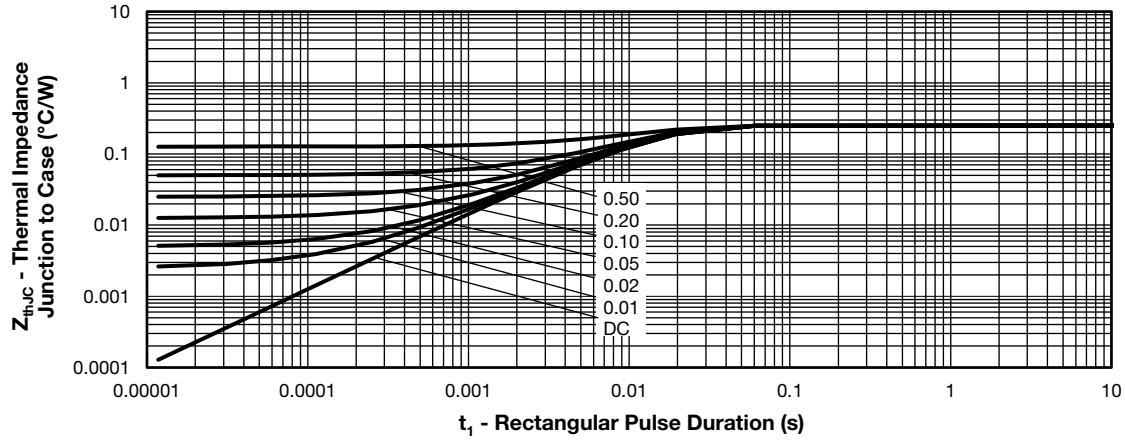


Fig. 34 - Z_{thJC} vs. t_1 Rectangular Pulse Duration (Maximum Thermal Impedance Z_{thJC} Characteristics - (Q2 - Q3 Trench IGBT))

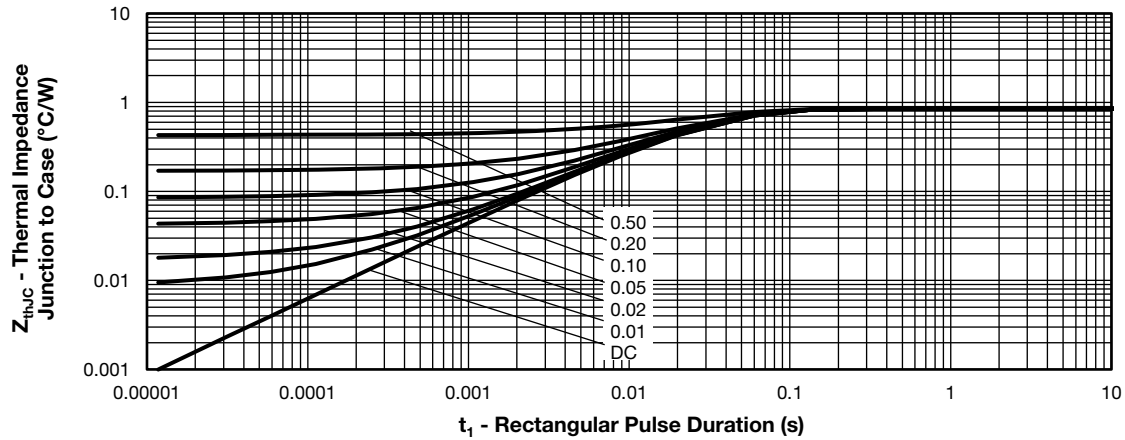


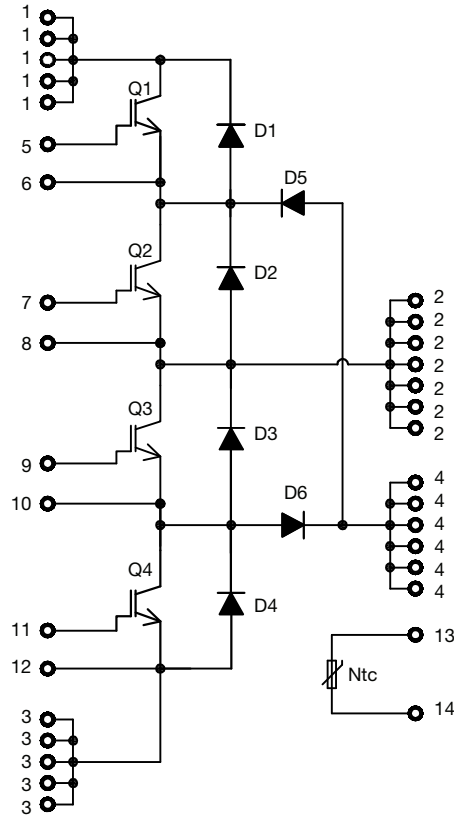
Fig. 35 - Z_{thJC} vs. t_1 Rectangular Pulse Duration (Maximum Thermal Impedance Z_{thJC} Characteristics - (D1 - D2 - D3 - D4 Antiparallel Diode))

ORDERING INFORMATION TABLE

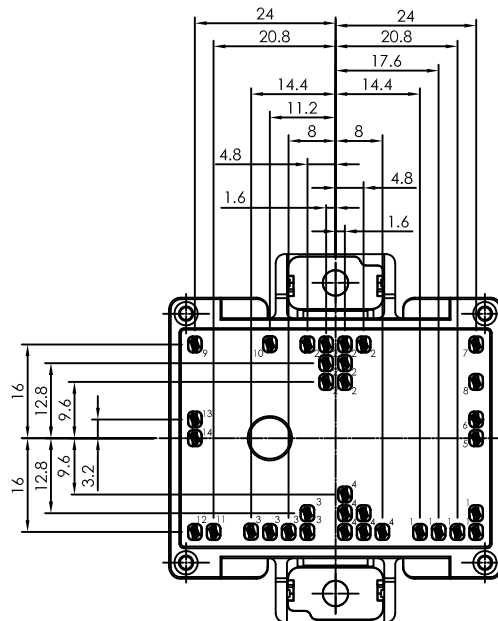
Device code	VS-	ET	F	150	Y	65	U
	①	②	③	④	⑤	⑥	⑦

- 1** - Vishay Semiconductors product
- 2** - Package indicator (ET = EMIPAK-2B)
- 3** - Circuit configuration (F = 3-levels half-bridge inverter stage)
- 4** - Current rating (150 = 150 A)
- 5** - Switch die technology (Y = trench IGBT)
- 6** - Voltage rating (65 = 650 V)
- 7** - Diode die technology (U = ultrafast diode)

CIRCUIT CONFIGURATION



PACKAGE in millimeters



LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95559
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