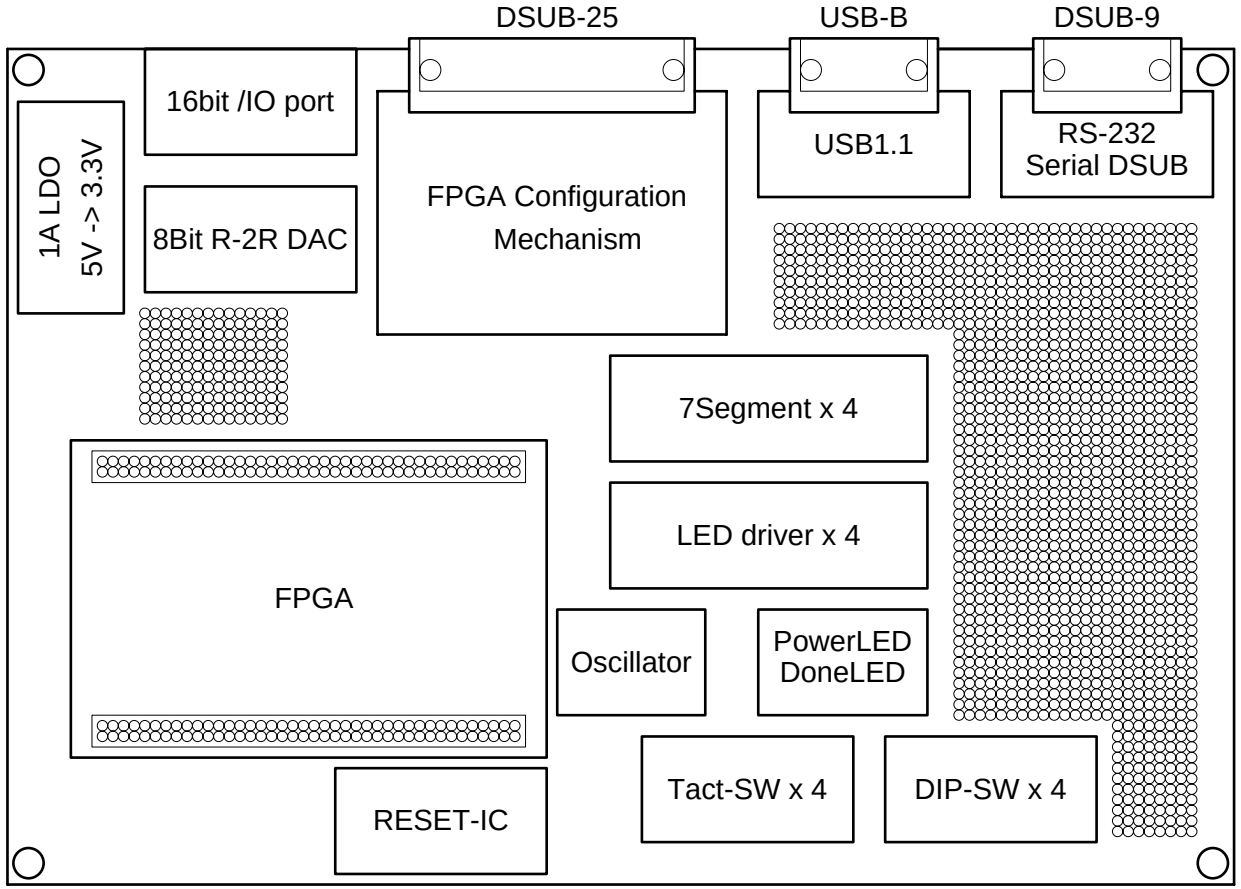
MFPGA-BASE Rev1.0

MARUTSU custom FPGA evaluation mother board.



LATTICE

CLK	1
RESET	1
7Segment	32
Tact-SW	4
DIP-SW	4
GPIO-IN	8
GPIO-OUT	8
DAC-ENB	1
UART	2
USB1.1	3
	64

XILINX

CLK	1
RESET	1
7Segment	32
Tact-SW	4
DIP-SW	4
GPIO-IN	4
GPIO-OUT	6
DAC-ENB	1
UART	2
USB1.1	3
	58

ALTERA

CLK	1
RESET	1
7Segment	32
Tact-SW	4
DIP-SW	4
GPIO-IN	4
GPIO-OUT	8
DAC-ENB	1
UART	2
USB1.1	3
	60

Designer:

Check:

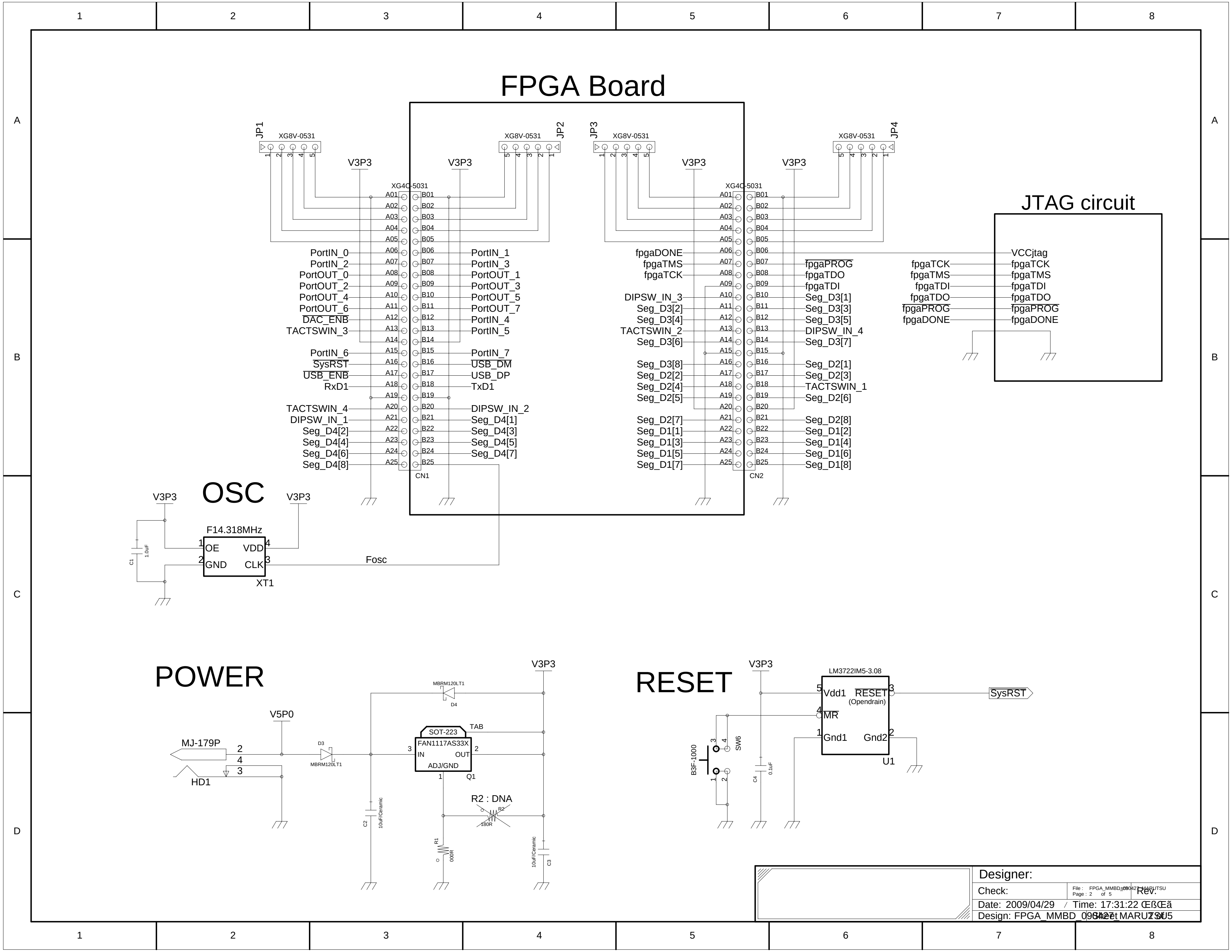
File : FPGA_MMBD_sch Page : 1 of 5 MARUTSU

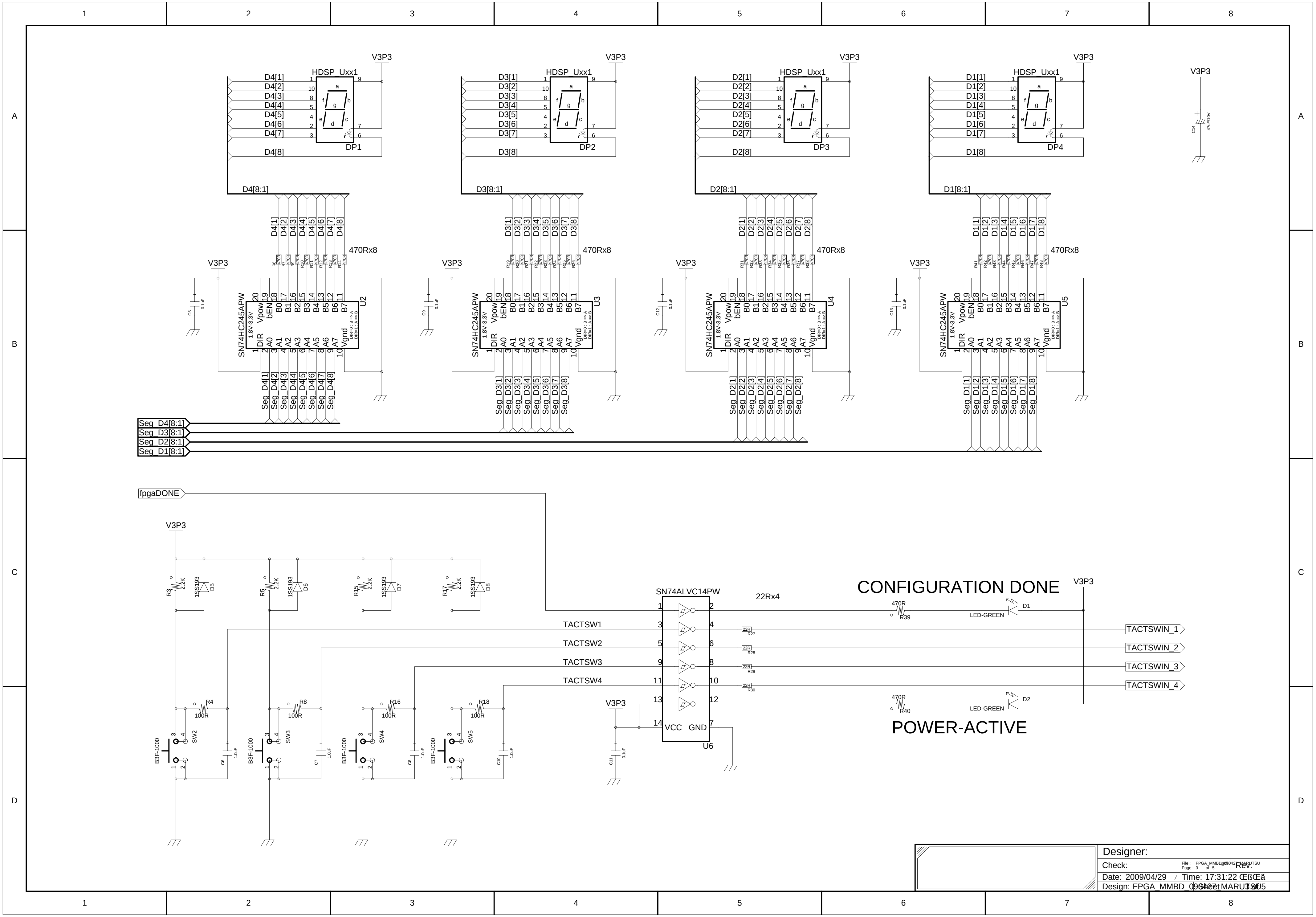
Rev.

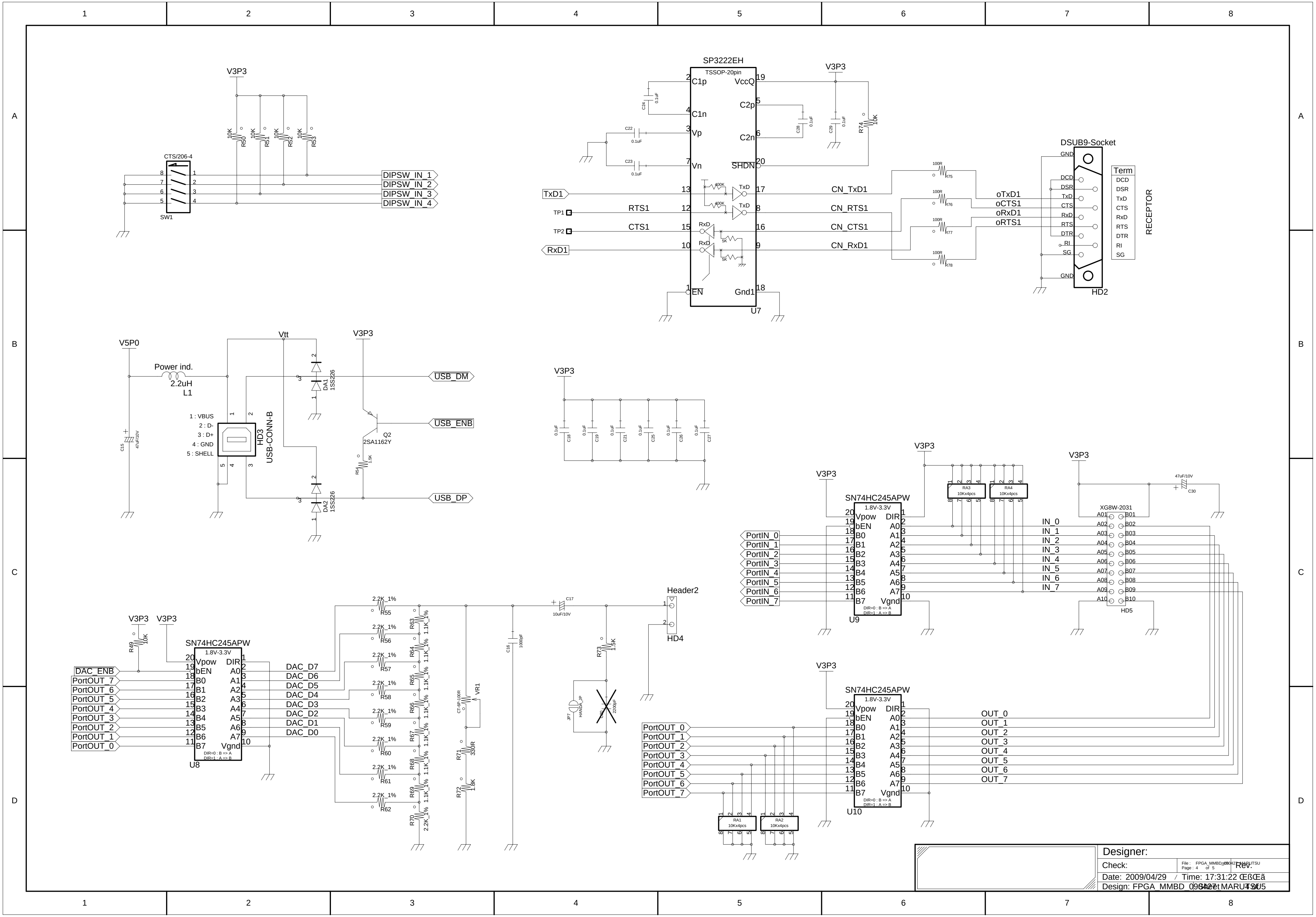
Date: 2009/04/29 / Time: 17:31:22

Design: FPGA_MMBD_090427

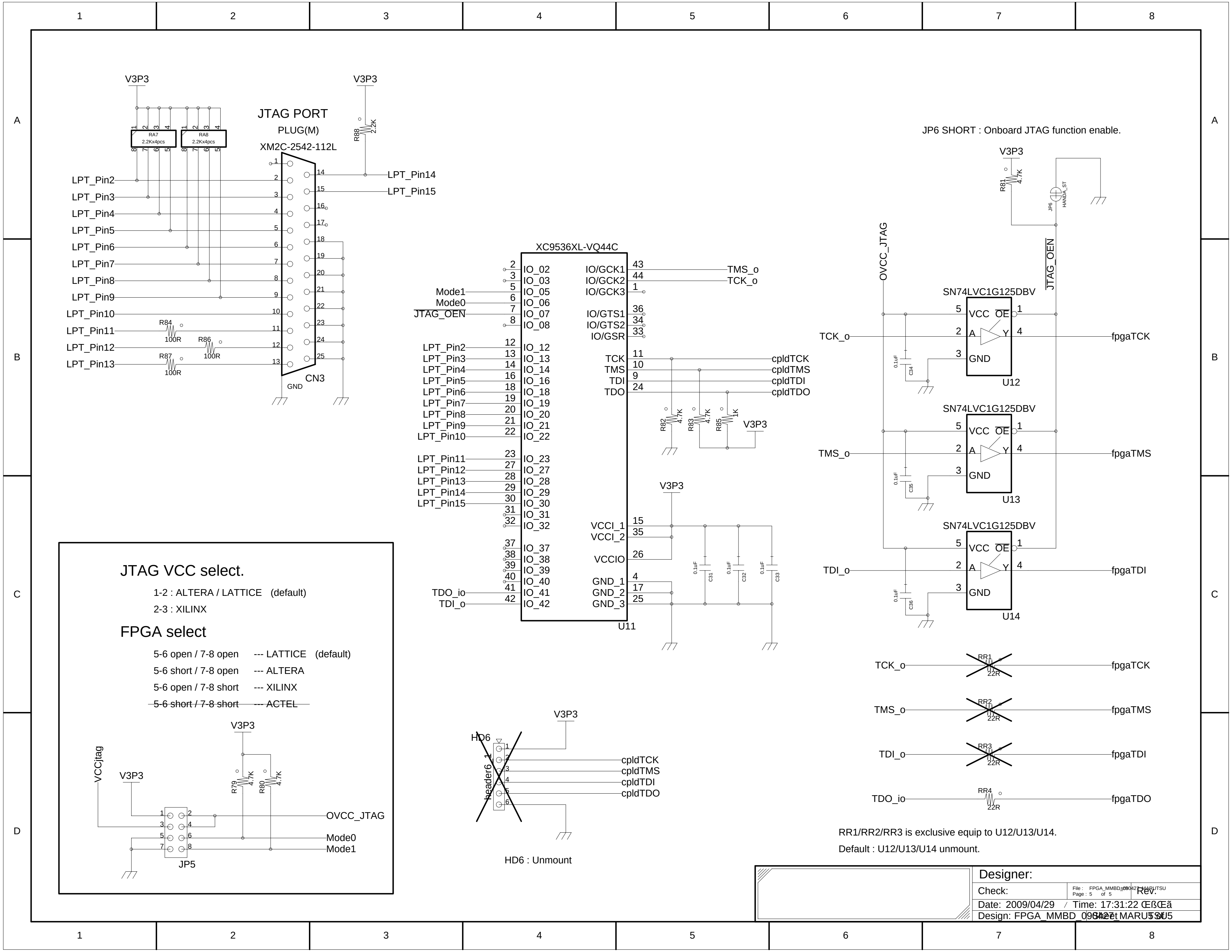
Sheet MARUTSU 1 of 5


FPGA Board
JP1
JP2
JP3
JP4
XG8V-0531
XG4C-5031
V3P3
CN1
CN2
PortIN_0
PortIN_1
PortIN_2
PortIN_3
PortOUT_0
PortOUT_1
PortOUT_2
PortOUT_3
PortOUT_4
PortOUT_5
PortOUT_6
PortOUT_7
DAC_ENB
PortIN_4
TACTSWIN_3
PortIN_5
PortIN_6
PortIN_7
SysRST
USB_DM
USB_ENB
USB_DP
RxD1
TxD1
TACTSWIN_4
DIPSW_IN_2
DIPSW_IN_1
Seg_D4[1]
Seg_D4[2]
Seg_D4[3]
Seg_D4[4]
Seg_D4[5]
Seg_D4[6]
Seg_D4[7]
Seg_D4[8]
fpgaDONE
fpgaTMS
fpgaPROG
fpgaTCK
fpgaTDO
fpgaTDI
DIPSW_IN_3
Seg_D3[1]
Seg_D3[2]
Seg_D3[3]
Seg_D3[4]
Seg_D3[5]
TACTSWIN_2
DIPSW_IN_4
Seg_D3[6]
Seg_D3[7]
Seg_D3[8]
Seg_D2[1]
Seg_D2[2]
Seg_D2[3]
Seg_D2[4]
TACTSWIN_1
Seg_D2[5]
Seg_D2[6]
Seg_D2[7]
Seg_D2[8]
Seg_D1[1]
Seg_D1[2]
Seg_D1[3]
Seg_D1[4]
Seg_D1[5]
Seg_D1[6]
Seg_D1[7]
Seg_D1[8]
JTAG circuit
VCCjtag
OSC
F14.318MHz
OE
VDD
GND
CLK
XT1
Fosc
C1
1.0uF
POWER
V5P0
MJ-179P
HD1
MBRM120LT1
D3
D4
SOT-223
FAN1117AS33X
IN
OUT
ADJ/GND
TAB
Q1
R2 : DNA
180R
R1
000R
C2
10uF/Ceramic
C3
RESET
LM3722IM5-3.08
Vdd1
RESET
(Opendrain)
MR
Gnd1
Gnd2
U1
SysRST
B3F-1000
SW6
C4
0.1uF
Designer:
Check:
Date: 2009/04/29
Time: 17:31:22
Design: FPGA_MMBD_090427_MARUTSU
Rev.
Page : 2 of 5


HDSP_Uxx1
DP1
DP2
DP3
DP4
V3P3
D4[8:1]
D3[8:1]
D2[8:1]
D1[8:1]
470Rx8
SN74HC245APW
U2
U3
U4
U5
Seg_D4[8:1]
Seg_D3[8:1]
Seg_D2[8:1]
Seg_D1[8:1]
fpgaDONE
SN74ALVC14PW
22Rx4
CONFIGURATION DONE
POWER-ACTIVE
TACTSW1
TACTSW2
TACTSW3
TACTSW4
TACTSWIN_1
TACTSWIN_2
TACTSWIN_3
TACTSWIN_4
LED-GREEN
D1
D2
R39
R40
470R
VCC
GND
U6
1SS193
B3F-1000
SW2
SW3
SW4
SW5
100R
2.2K
Designer:
Check:
Rev.
Date: 2009/04/29
Time: 17:31:22
Design: FPGA_MMBD_09



V3P3
CTS/206-4
SW1
R50 10K
R51 10K
R52 10K
R53 10K
DIPSW_IN_1
DIPSW_IN_2
DIPSW_IN_3
DIPSW_IN_4
SP3222EH
TSSOP-20pin
C1p
C1n
Vp
Vn
VccQ
C2p
C2n
SHDN
EN
Gnd1
U7
TxD1
RxD1
TP1
TP2
RTS1
CTS1
CN_TxD1
CN_RTS1
CN_CTS1
CN_RxD1
R74 10K
R75 100R
R76 100R
R77 100R
R78 100R
oTxD1
oCTS1
oRxD1
oRTS1
DSUB9-Socket
HD2
Term
DCD
DSR
TxD
CTS
RxD
RTS
DTR
RI
SG
GND
RECEPTOR
V5P0
Vtt
Power ind.
2.2uH
L1
1 : VBUS
2 : D-
3 : D+
4 : GND
5 : SHELL
HD3
USB-CONN-B
DA1 1SS226
DA2 1SS226
USB_DM
USB_ENB
USB_DP
Q2
2SA1162Y
R54 1.5K
C15 47uF/10V
C18 C19 C21 C25 C26 C27 0.1uF
SN74HC245APW
1.8V-3.3V
Vpow
bEN
DIR
Vgnd
DIR=0 : B => A
DIR=1 : A => B
U8
U9
U10
DAC_ENB
PortOUT_7
PortOUT_6
PortOUT_5
PortOUT_4
PortOUT_3
PortOUT_2
PortOUT_1
PortOUT_0
DAC_D7
DAC_D6
DAC_D5
DAC_D4
DAC_D3
DAC_D2
DAC_D1
DAC_D0
R49 10K
R55–R62 2.2K_1%
R63–R69 1.1K_1%
R70 2.2K_1%
VR1
R71 330R
R72 1.8K
R73 1.5K
C16 1000pF
C17 10uF/10V
JP7 HANDA_JP
Header2
HD4
PortIN_0
PortIN_1
PortIN_2
PortIN_3
PortIN_4
PortIN_5
PortIN_6
PortIN_7
IN_0
IN_1
IN_2
IN_3
IN_4
IN_5
IN_6
IN_7
OUT_0
OUT_1
OUT_2
OUT_3
OUT_4
OUT_5
OUT_6
OUT_7
RA1 RA2 RA3 RA4 10Kx4pcs
XG8W-2031
HD5
C30 47uF/10V
Designer:
Check:
Rev.
Date: 2009/04/29
Time: 17:31:22
Design: FPGA_MMBD_090427
Sheet 4 of 5



JTAG PORT
PLUG(M)
XM2C-2542-112L
CN3
GND
V3P3
RA7 2.2Kx4pcs
RA8 2.2Kx4pcs
R88 2.2K
LPT_Pin2
LPT_Pin3
LPT_Pin4
LPT_Pin5
LPT_Pin6
LPT_Pin7
LPT_Pin8
LPT_Pin9
LPT_Pin10
LPT_Pin11
LPT_Pin12
LPT_Pin13
LPT_Pin14
LPT_Pin15
R84 100R
R86 100R
R87 100R
XC9536XL-VQ44C
U11
IO_02
IO_03
IO_05
IO_06
IO_07
IO_08
IO_12
IO_13
IO_14
IO_16
IO_18
IO_19
IO_20
IO_21
IO_22
IO_23
IO_27
IO_28
IO_29
IO_30
IO_31
IO_32
IO_37
IO_38
IO_39
IO_40
IO_41
IO_42
IO/GCK1
IO/GCK2
IO/GCK3
IO/GTS1
IO/GTS2
IO/GSR
TCK
TMS
TDI
TDO
VCCI_1
VCCI_2
VCCIO
GND_1
GND_2
GND_3
Mode1
Mode0
JTAG_OEN
TDO_io
TDI_o
TMS_o
TCK_o
cpldTCK
cpldTMS
cpldTDI
cpldTDO
R82 4.7K
R83 4.7K
R85 1K
C31 0.1uF
C32 0.1uF
C33 0.1uF
JP6 SHORT : Onboard JTAG function enable.
R81 4.7K
JP6 HANDA_ST
OVCC_JTAG
JTAG_OEN
SN74LVC1G125DBV
VCC
OE
A
Y
GND
U12
U13
U14
C34 0.1uF
C35 0.1uF
C36 0.1uF
fpgaTCK
fpgaTMS
fpgaTDI
fpgaTDO
RR1 22R
RR2 22R
RR3 22R
RR4 22R
RR1/RR2/RR3 is exclusive equip to U12/U13/U14.
Default : U12/U13/U14 unmount.
JTAG VCC select.
1-2 : ALTERA / LATTICE (default)
2-3 : XILINX
FPGA select
5-6 open / 7-8 open --- LATTICE (default)
5-6 short / 7-8 open --- ALTERA
5-6 open / 7-8 short --- XILINX
5-6 short / 7-8 short --- ACTEL
VCCjtag
R79 4.7K
R80 4.7K
JP5
OVCC_JTAG
Mode0
Mode1
HD6
header6
HD6 : Unmount
Designer:
Check:
Rev.
File : FPGA_MMBD_090427
Page : 5 of 5
Date: 2009/04/29
Time: 17:31:22
Design: FPGA_MMBD_090427